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Ka-Band GaAs FET Monolithic Power Amplifier Development

Paul Saunier and Hua Quen Tserng
Texas Instruments Incorporated
Dallas, Texas

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Space Administration

FINAL TECHNICAL PROGRESS
FOR
Ka-BAND GaAs FET MONOLITHIC
POWER AMPLIFIER DEVELOPMENT
CONTRACT NO. NAS3-24239

Prepared for
NASA Lewis Research Center
Cleveland, OH 44135

Prepared by
Texas Instruments Incorporated
Central Research Laboratories
P.O. Box 655936, M.S. 105
Dallas, TX 75265

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FOR
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ABSTRACT

Over the course of this program, very extensive progress was made in Ka-band GaAs technology. At the beginning of the program, odd-shaped VPE MESFET wafers were used. A breakthrough in power and efficiency was achieved with highly doped (8×10^{17} cm^{-3}) MBE grown MESFET material. We obtained power of 112 mW with 16 dB gain and 21.6% efficiency at 34 GHz with a monolithic 50-100-250 μm amplifier. The next breakthrough came with the use of heterostructures grown by MBE (AlGaAs/InGaAs where the InGaAs is highly doped). This allowed us to achieve high power density with high efficiency. A benchmark 40% efficiency was achieved with a single-stage 100 μm MMIC at 32.5 GHz. The corresponding three-stage 50-100-250 μm amplifier achieved 180 mW with 23 dB gain and 30.3% efficiency.

The next breakthrough came with 3-inch MBE grown PHEMT wafers incorporating an etch-stop layer for the gate recess (using RIE). Again, state-of-the-art performances were achieved: 40% efficiency with 235 mW output power and 20.7 dB gain. The single-stage 2×600 μm chip demonstrated 794 mW output power with 5 dB gain and 38.2% power-added efficiency (PAE).

The Ka-band technology developed under this program has promise for extensive use: JPL demonstrated 32 GHz phased arrays with a three-stage amplifier developed under this contract. A variation of the three-stage amplifier was used successfully in a 4×4 phased array transmitter developed under another NASA contract.

EXECUTIVE SUMMARY

Over the course of this program, very extensive progress was made in Ka-band GaAs technology. At the beginning of the program, odd-shaped VPE MESFET wafers were used. A breakthrough in power and efficiency was achieved with highly doped (8×10^{17} cm^{-3}) MBE grown MESFET material. We obtained power of 112 mW with 16 dB gain and 21.6% efficiency at 34 GHz with a monolithic 50-100-250 μm amplifier. The next breakthrough came with the use of heterostructures grown by MBE (AlGaAs/InGaAs where the InGaAs is highly doped). This allowed us to achieve high power density with high efficiency. A benchmark 40% efficiency was achieved with a single-stage 100 μm MMIC at 32.5 GHz. The corresponding three-stage 50-100-250 μm amplifier achieved 180 mW with 23 dB gain and 30.3% efficiency.

The next breakthrough came with 3-inch MBE grown PHEMT wafers incorporating an etch-stop layer for the gate recess (using RIE). Again, state-of-the-art performances were achieved: 40% efficiency with 235 mW output power and 20.7 dB gain. The single-stage 2×600 μm chip demonstrated 794 mW output power with 5 dB gain and 38.2% power-added efficiency (PAE).

We consider this contract to be one of the most successful and valuable programs for TI. The Ka-band technology developed under this contract has promise for extensive use.

Under the NASA Ka-MIST contract, TI developed a 4×4 phased array transmitter that incorporates sixteen 50-100-350 μm amplifiers capable of 180 to 200 mW output power at 30 GHz. These chips were modifications of the amplifiers developed under this contract. Experiments conducted by NASA demonstrated successful communication between aircraft and ground station via the ACTS satellite. These tests were reported in *Aviation Week.*

TI developed, in an important internal project, a medium- and a high-power amplifier at 27 to 28 GHz. These amplifiers are based on the 100-200-400 μm and 600-1200 μm amplifiers developed under this contract. The first-pass design achieved excellent performance results. The high-power amplifier (400-600-2400 μm) achieved 1.15 W with 20.6 dB gain and 37% power-added efficiency (PAE) at 27 GHz. The medium-power amplifier (100-200-400 μm) achieved 300 mW with 24 dB gain and 40% PAE.

The same technology will be extended to our MILSATCOM program, which requires both medium-power (250 mW) and high-power (0.5 W) amplifiers at 44 GHz.

Potentially large communication programs such as TELEDESIC using LEO satellites would use transmitters at Ka-band such as those developed on this contract.

Numerous publications resulted from the work developed under this program, as follows:

"High-performance Ka-band power field-effect transistors," B. Kim, P. Saunier, and H.D. Shih. GOMAC-86, San Diego, California.

"A high-efficiency Ka-band monolithic GaAs FET amplifier," P. Saunier, H.Q. Tserng, N. Camilleri, K. Bradshaw, and H.D. Shih. *Proceedings of the 1988 IEEE GaAs IC Symposium,* Nashville, Tennessee, pp. 37, 39 (November 6-9, 1988).

"AlGaAs/InGaAs heterostructures with doped channels for discrete devices and monolithic amplifiers," P. Saunier and H.Q. Tserng. *IEEE Transactions on Electron Devices,* Vol. 36, No. 10 (October 1989).

"Doped channel heterostructures for millimeter-wave discrete devices and MMICs." *Conference Record, 1989 IEEE Military Communication Conference,* pp. 730-734 (October 1989).

"Millimeter-wave power transistors and circuits," H.Q. Tserng, B. Kim, P. Saunier, H.D. Shih, and M.A. Khatibzadeh. *Microwave Journal,* pp. 125-135 (April 1989).

"Advances in power MMIC amplifier technology in space communication," H.Q. Tserng. *SPIE,* Vol. 1475, Monolithic Microwave Integrated Circuits for Sensors, Radars, and Communication Systems (1991).

"A high-efficiency Ka-band monolithic pseudomorphic HEMT amplifier," P. Saunier, H.Q. Tserng, and Y.C. Kao. *SPIE,* Vol. 1475, Monolithic Microwave Integrated Circuits for Sensors, Radars, and Communication Systems (1991).

"High-efficiency, high-gain monolithic heterojunction FET amplifier at 31 GHz," H.Q. Tserng. *Electronics Letters,* Vol. 29, No. 3, pp. 304-306 (1993).

"GaAs power MMIC amplifiers: recent advances." 3rd International Conference on VLSI and CAD (ICVC'93), Taejon, Korea (November 15-17, 1993).

"Fabrication and performance of pHEMT Ka-band three-stage amplifiers for phased-array application," P. Saunier. SPIE Conference on Millimeter and Sub-Millimeter Wave Applications, San Jose, California (1993).

SECTION I
INTRODUCTION

The objective of this program is to demonstrate the feasibility of a high power, high efficiency, high gain, narrow (5%) bandwidth monolithic GaAs FET amplifier in the 20 to 35 GHz frequency range for advanced communications applications. Originally, three amplifier modules were to be developed: one at a center frequency of 23 GHz, one at 29 GHz, and one at 32.5 GHz. The bandwidth is 5% with greater than 15 dB RF gain at 1 dB compression. The output power (1 dB compression) goals were 1, 0.4, and 0.25 W at 23, 29, and 32.5 GHz, respectively. The PAE goals were 25% at 23 GHz and 20% at 29 GHz and 32.5 GHz. In April 1986, the program was modified to delete the 28 GHz task and include a 32.5 GHz high electron mobility transistor (HEMT) amplifier with a goal of 100 mW power, 20 dB gain, and 35% PAE. In March 1990, the program was again modified with the following new goals for the 32.5 GHz monolithic amplifiers:

- 250 mW with ≥15 dB gain and ≥50% PAE
- 1 W with ≥10 dB gain and ≥35% PAE.

Table 1 summarizes the frequency, gain, power, and efficiency of the amplifier to be developed.

Table 1.
Amplifier Development Requirements Summary

	Frequency (GHz)	Gain (dB)	Power (W)	Efficiency (%)
Initial Program	23	15	1	25
	29	15	0.4	20
	32.5	15	0.25	20
Modification 1	32.5	20	0.1	35
Modification 2	32.5	15	0.25	≥50
	32.5	10	1	≥35

SECTION II
23 GHz AMPLIFIER DESIGN AND FABRICATION

The block diagram of the amplifier is shown in Figure 1. The 300-900-2400 μm gate width FETs are cascaded to achieve 1 W output power with 15 dB gain. The gain allocations for each stage are shown. In order to characterize more readily the input, output, and interstage matching networks of the amplifier, we designed 300 μm single stage and 300-900 μm two-stage submodules using two different configurations.

One design has highpass filters (transmission and inductor to ground) for the input of the first, second, and third stages. In a second design, a highpass filter is used for the input of the first stage, and lowpass filters (transmission line and capacitor to ground) are used for the second and third stages. Two first-stage modules were considered, with the same input match, but with inductor to ground and capacitor to ground, respectively, to match the FET output. Figures 2 and 3 show digitized plots of the amplifiers. Several lots of MBE and MOCVD devices were processed. The first MBE lot had a 2.5×10^{17} doping level. Figures 4 through 6 show, respectively, the three-stage amplifiers with shunt inductance to ground and capacitor to ground matching circuits; the two-stage amplifiers with shunt inductance to ground and capacitor to ground matching circuits; and the single-stage amplifier, also with inductance to ground and capacitor to ground matching circuits. The dc characteristics of a 300 μm device (one-stage) are shown in Figure 7. The pinchoff voltage is 5 V, I_{dss} is 145 mA, and the transconductance is 130 mS/mm.

Figure 8 shows the gain response of a one-stage amplifier with inductor to ground. The input power is 10 dBm. The gain achieved is 7 dB at 22.5 GHz with 6.5 V on the drain. All two-stage amplifiers with inductor to ground were shorted because of misalignment of the wide recess, an error in the e-beam program that has since been corrected. The three-stage amplifier with inductor to ground has a maximum small-signal gain of 13 dB at 21 GHz. The output is matched at 19 GHz and requires tuning to operate at 21 GHz. The one-stage amplifier with capacitor to ground has a small-signal gain of 7 dB at 25 GHz with 5.5 V on the drain. Figure 9 shows the gain response with 10 dBm input power. The amplifier has 4.6 dB gain with 22.2 dBm output power (166 mW)

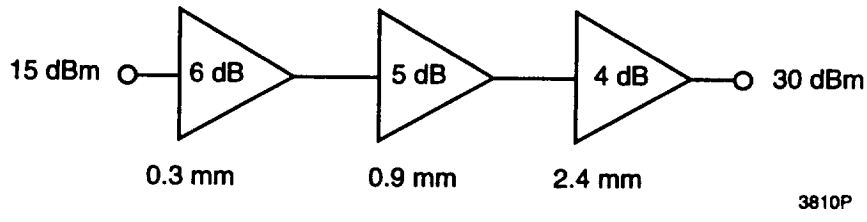


Figure 1. Block diagram of the 23 GHz amplifier.

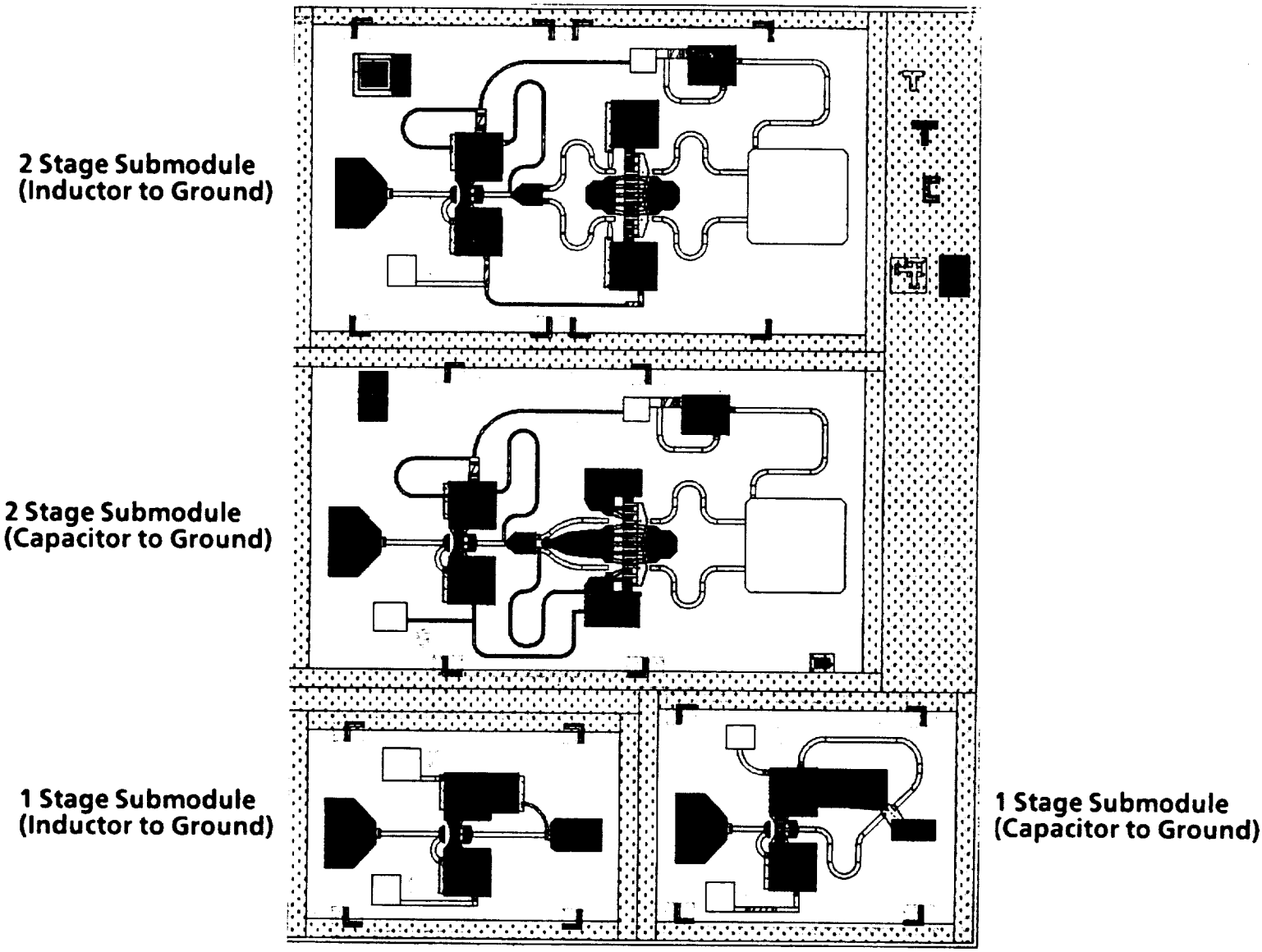
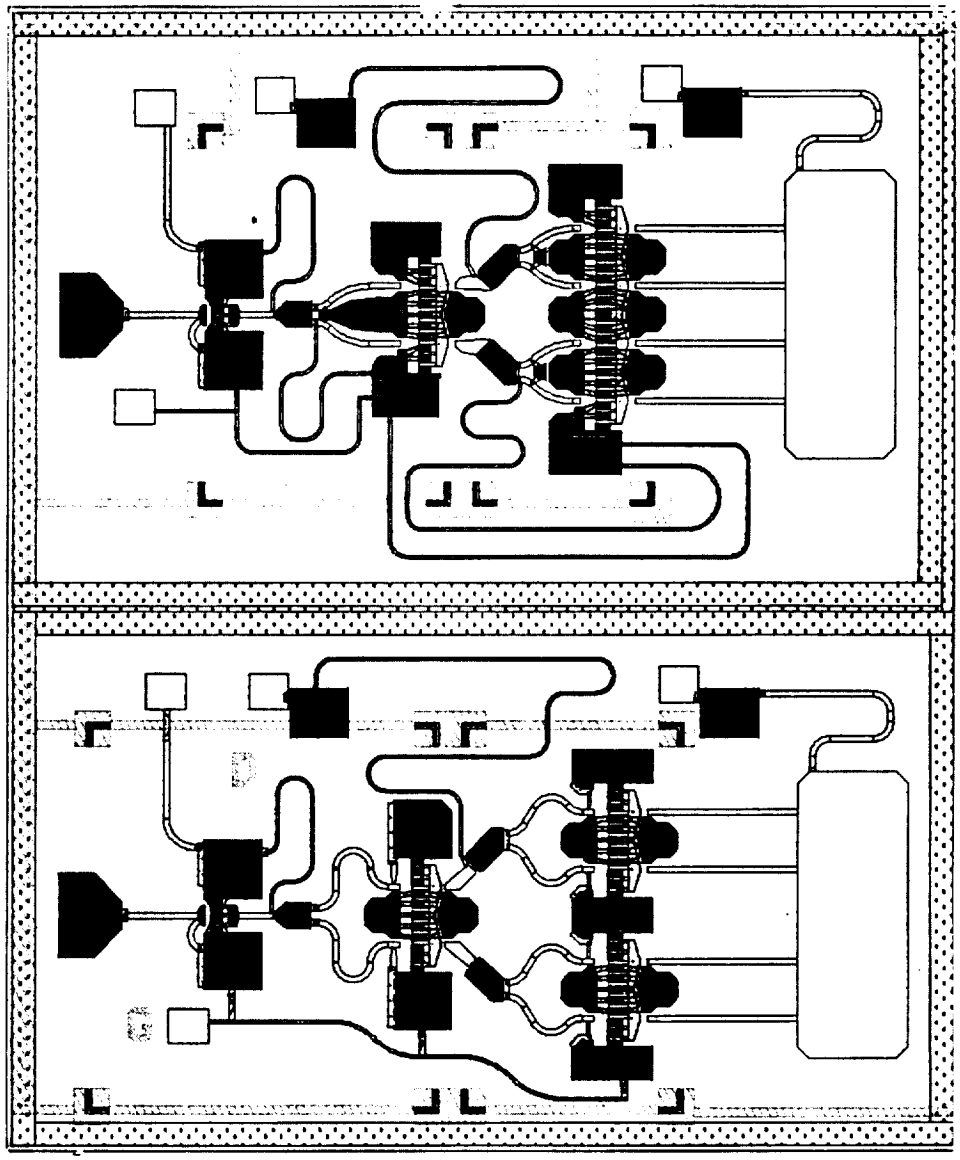


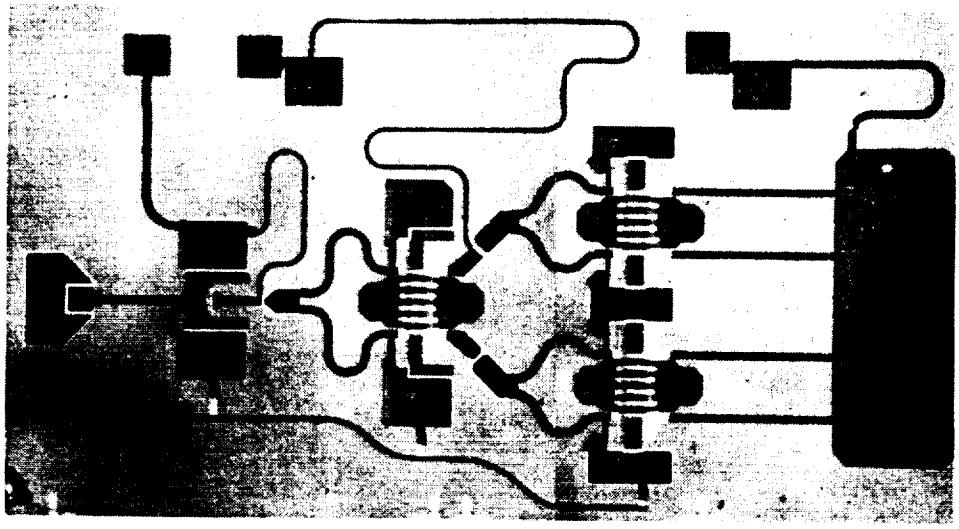
Figure 2. Digitized plots of 23 GHz submodules.

3 Stage Module
(Capacitor to Ground)

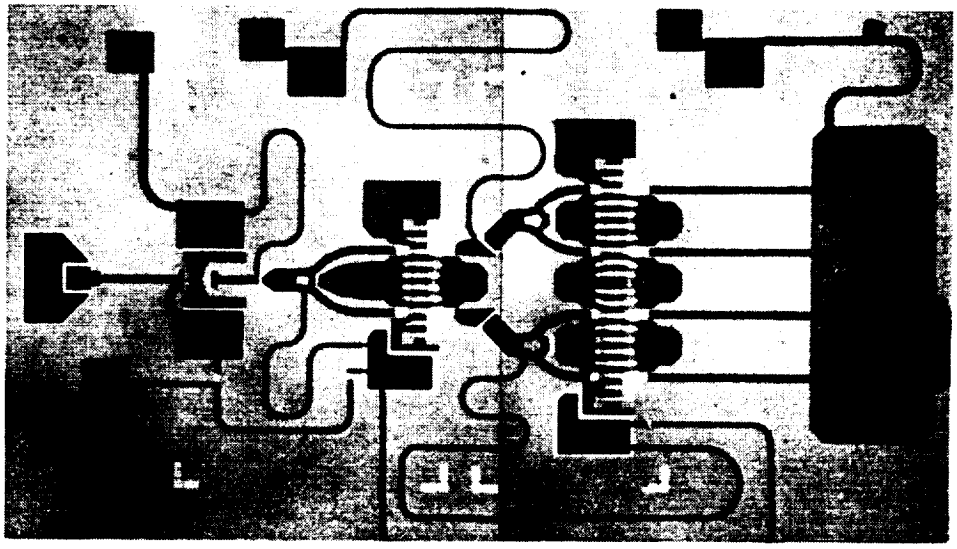


3 Stage Module
(Inductor to Ground)

Figure 3. Digitized plot of 23 GHz amplifier.

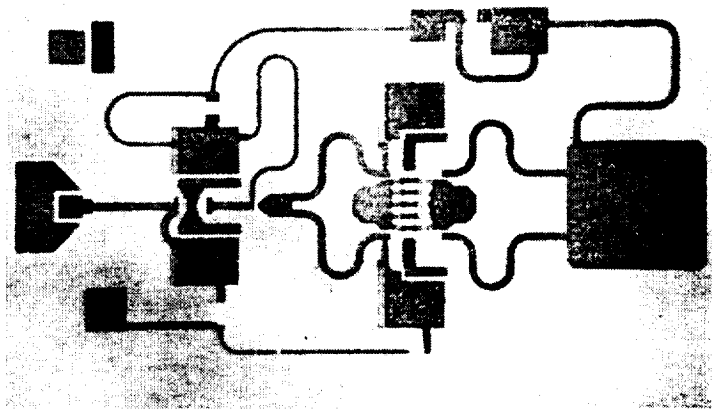


(a)

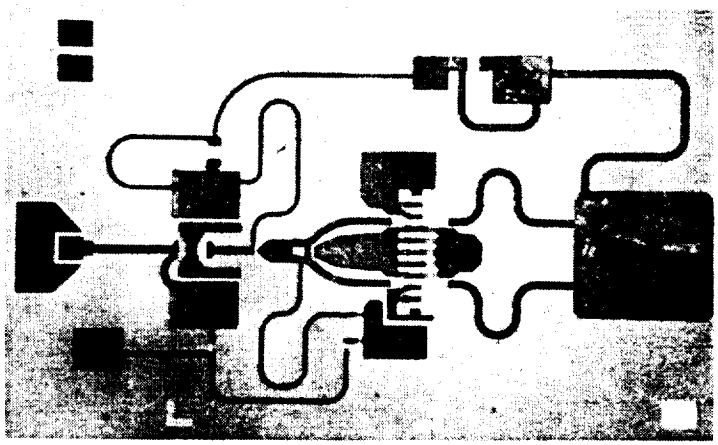


(b)

Figure 4. 23 GHz, three-stage amplifier with (a) shunt inductor to ground, and (b) shunt capacitor to ground.

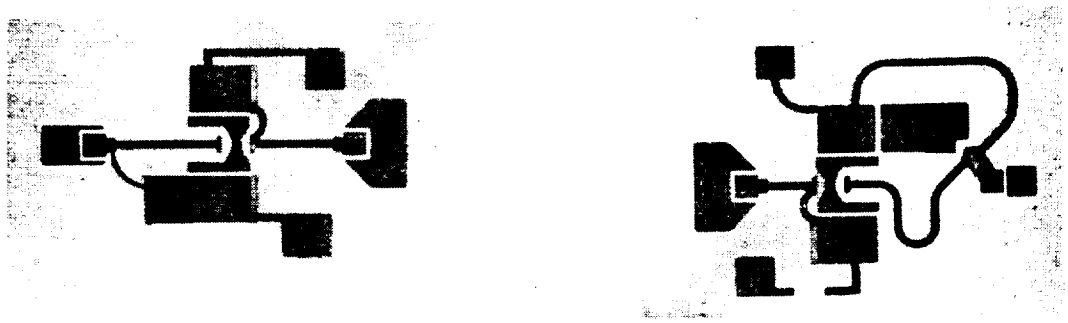


(a)



(b)

Figure 5. 23 GHz, two-stage amplifier with (a) shunt inductor to ground, and (b) shunt capacitor to ground.



(a) (b)

Figure 6.
23 GHz, one-stage amplifier with (a) shunt inductor to ground, and (b) shunt capacitor to ground.

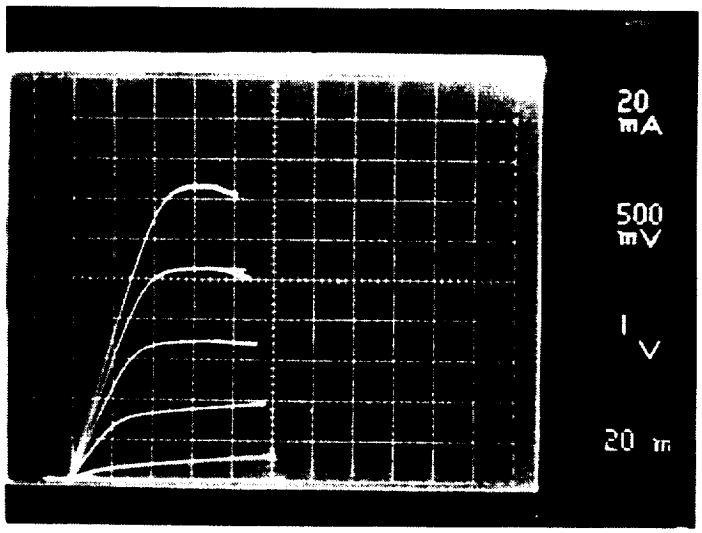


Figure 7.
The dc characteristics of a 300 μm, 23 GHz one-stage amplifier.

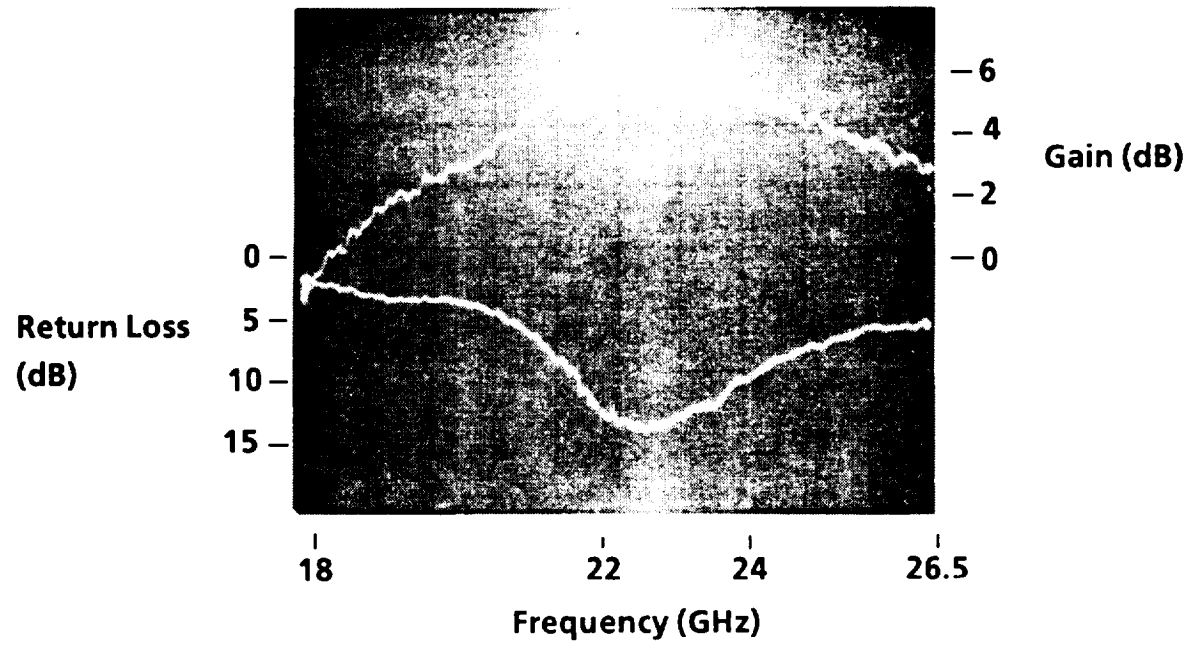


Figure 8. Gain-frequency response of a one-stage amplifier with inductor to ground. Does not include 0.8 dB fixture loss.

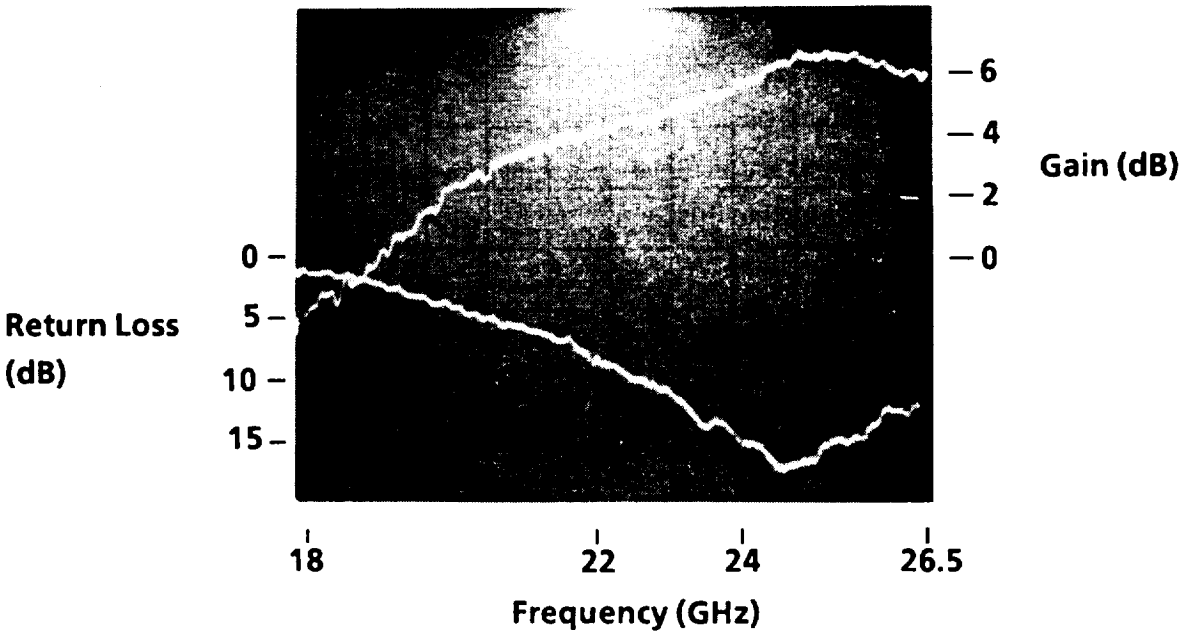


Figure 9. Gain-frequency response of a one-stage amplifier with capacitor to ground (input power = 10 dBm). Does not include 0.8 dB fixture loss.

and 15% PAE (Figure 10). Maximum power under full compression is 200 mW (power density of 0.7 W/mm). The two-stage amplifier with capacitor to ground has 9 dB gain with 15 dBm input power at 24 GHz (Figure 11). The output, however, is matched too low and needs to be chip-tuned. The output of the three-stage amplifier with capacitor to ground is matched at 19 GHz (Figure 12). Placing a strap in the output moves the match to 23 GHz, which produces a 15 dB gain with 10 dBm input power. The amplifier is capable of 28.5 dBm output power (700 mW) with 10.9 dB gain at 23.5 GHz when pushed into compression.

Chips from the following lot of MBE slices had lower performance. The pinchoff voltage was too high (6 V) for optimum performance, and the yield was low because of poor e-beam gate exposure; no good three-stage amplifier was found.

The best results were achieved with a lot of MOCVD wafers doped at 3.5×10^{17}. The gate lengths on the chips were less than 0.3 μm. The dc yields for the one-stage, two-stage, and three-stage amplifiers were 67%, 33%, and 36%, respectively. Extensive testing was performed and the results are summarized below:

One-Stage Amplifier (Capacitor to Ground)

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–0.75	10.5	11
9.25	8	—
14.25	—	5-5

The maximum gain is obtained at 23 GHz, and very little tuning on the input or output is required to optimize the performance. Figure 13 shows the gain-frequency response of the amplifier with 0 dBm input power and no tuning.

Two-Stage Amplifier (Capacitor to Ground)

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–0.75	16.5	17.5
9.25	13	14
14.25	9.5	10.5

The maximum gain under power conditions is obtained at a slightly low frequency (22.2 GHz), and very little tuning is required for optimum output power. The amplifier is capable of 300 mW output power with 10.5 dB gain and 13% PAE. Figure 14 shows the amplifier gain-frequency response (with tuning) with 14.25 dBm input power. The marker is at 23 GHz.

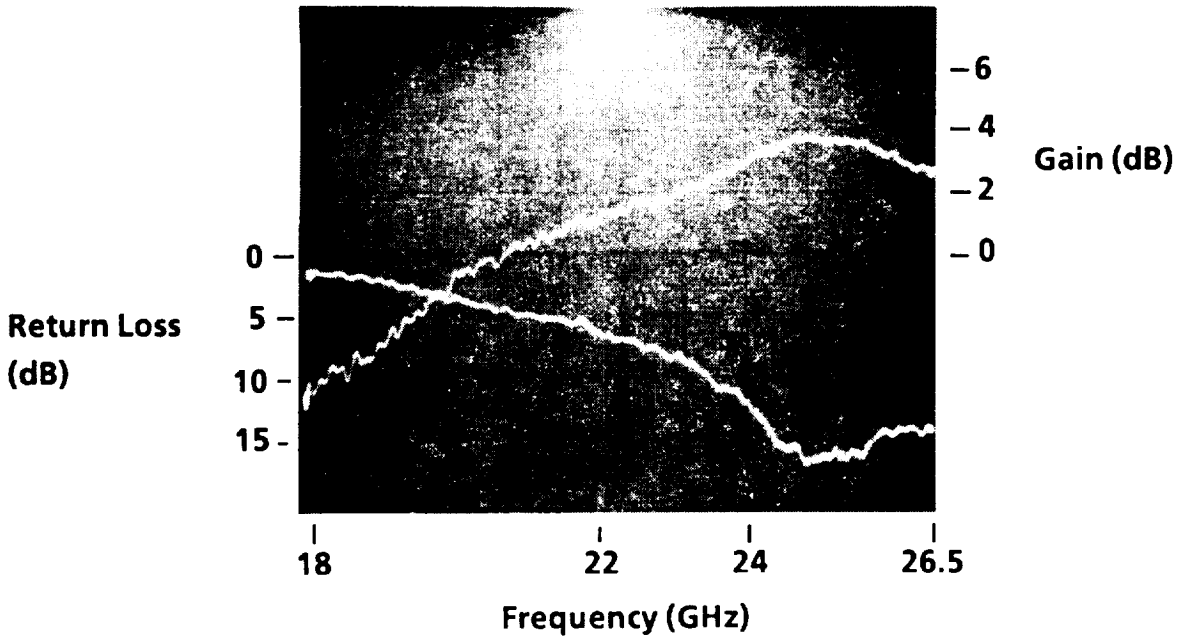


Figure 10. Gain-frequency response of a one-stage amplifier with capacitor to ground (input power = 17.6 dBm). Does not include 0.8 dB fixture loss.

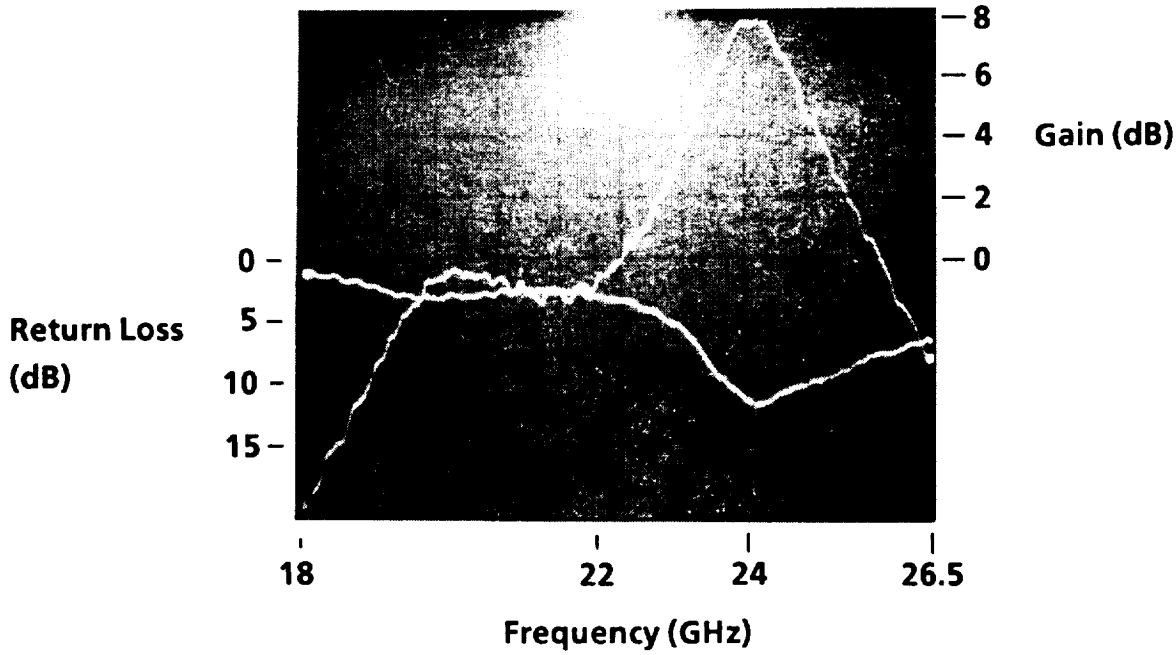


Figure 11. Gain-frequency response of a two-stage amplifier with capacitor to ground (input power = 15 dBm). Does not include 0.8 dB fixture loss.

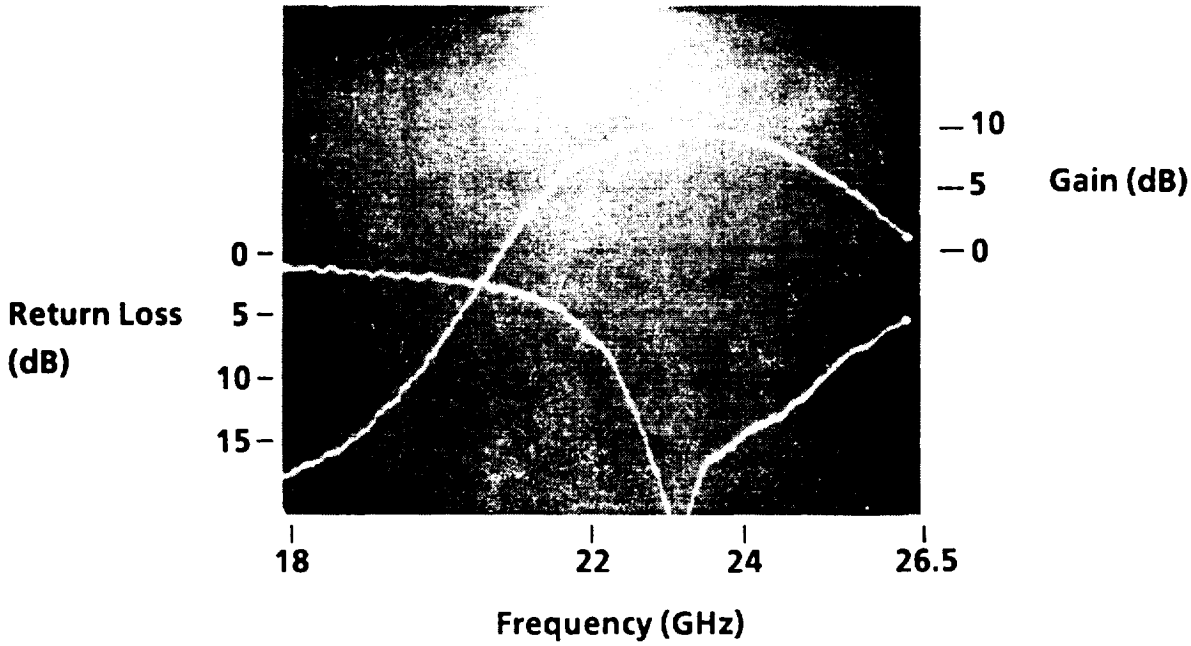


Figure 12. Gain-frequency response of a three-stage amplifier with capacitor to ground (input power = 18 dBm). Does not include 0.8 dB fixture loss.

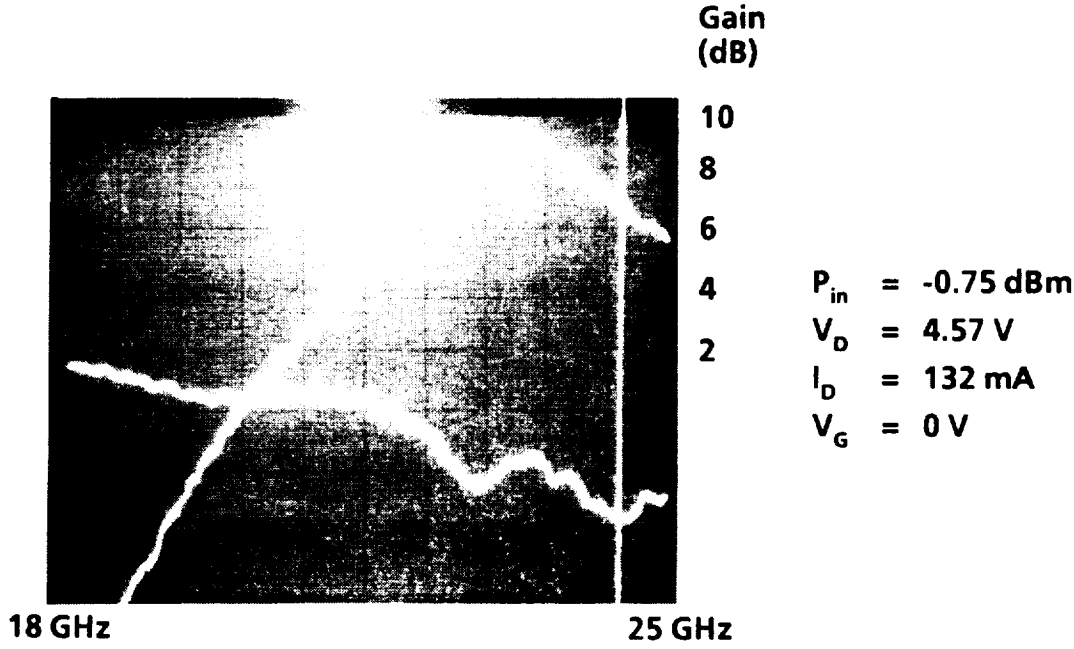


Figure 13. Gain-frequency response of a one-stage amplifier with capacitor to ground, no tuning.

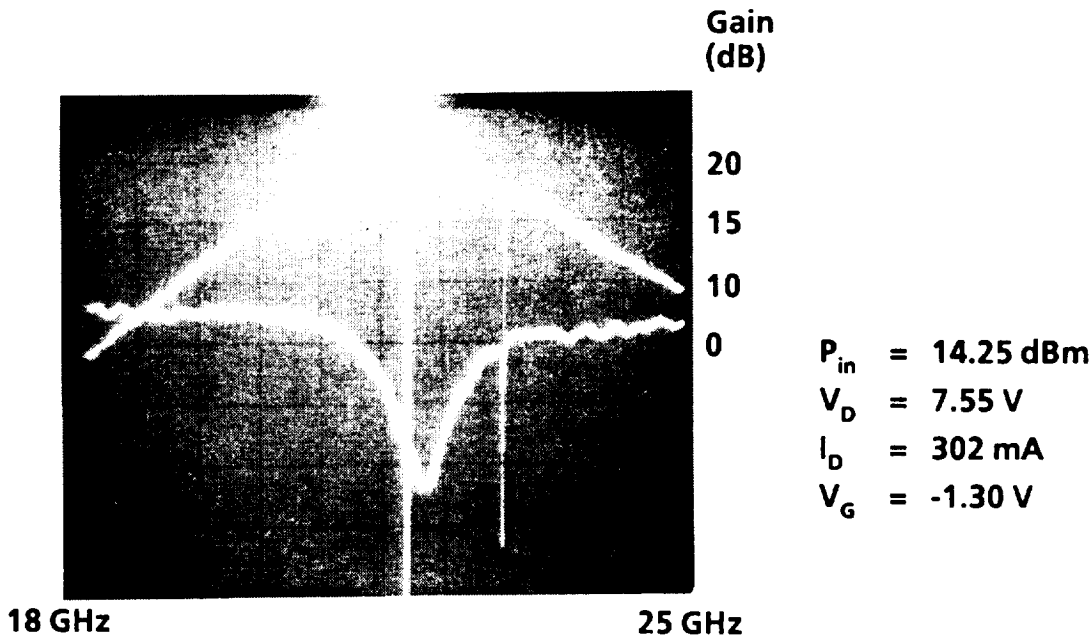


Figure 14. Gain-frequency response of a two-stage amplifier with capacitor to ground, with tuning.

Three-Stage Amplifier (Capacitor to Ground)

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–0.75	13.5	16.5
14.25	—	10

The gain is too low, particularly in view of the results obtained with the two-stage amplifier. This indicates that the interstage matching between stages two and three needs to be optimized. Figure 15 shows the amplifier gain-frequency response with –0.75 dBm input power and no tuning.

One-Stage Amplifier (Inductor to Ground)

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–0.75	8.5	9.5
9.25	5	7.75
15.5	—	5.25

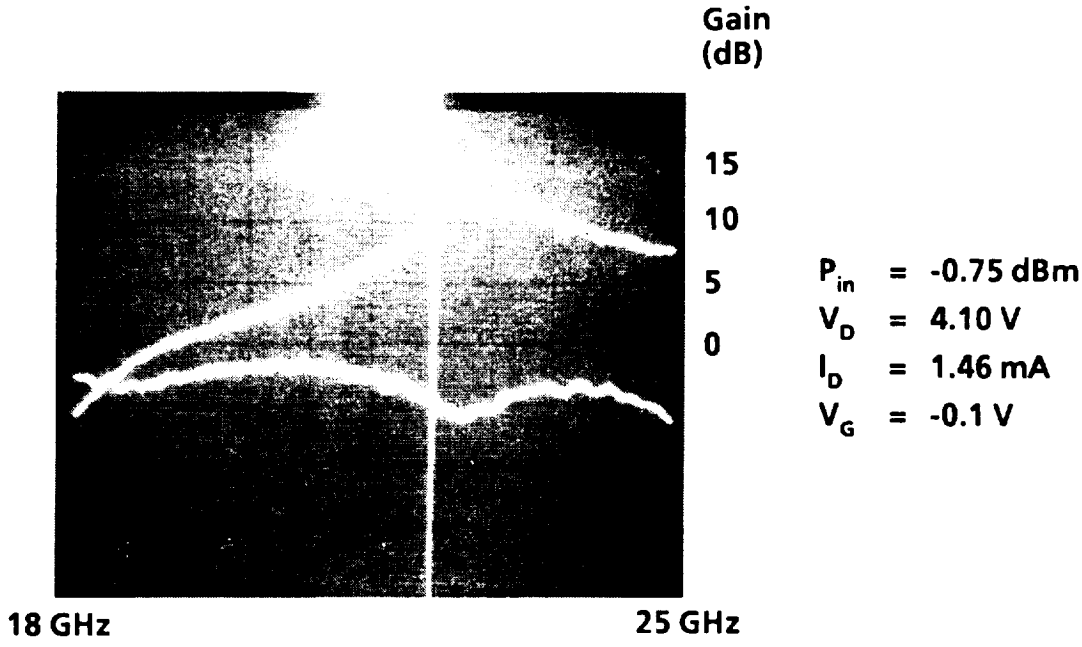


Figure 15. Gain-frequency response of a three-stage amplifier with capacitor to ground, no tuning.

The amplifier requires input and output tuning to perform optimally at 23 GHz. It is then capable of 120 mW output power with 5.25 dB gain and 15% PAE. Figure 16 shows the gain-frequency response of the amplifier under these conditions.

Two-Stage Amplifier (Inductor to Ground)

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–0.75	15.5	17.5
9.25	—	12.75

Figure 17 shows the amplifier gain-frequency response with 9.25 dBm input power. This two-stage amplifier does not perform as well as the two-stage amplifier with capacitor to ground.

Two-Stage Amplifier (Inductor to Ground)

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–0.75	15.5	17.5
9.25	—	12.75

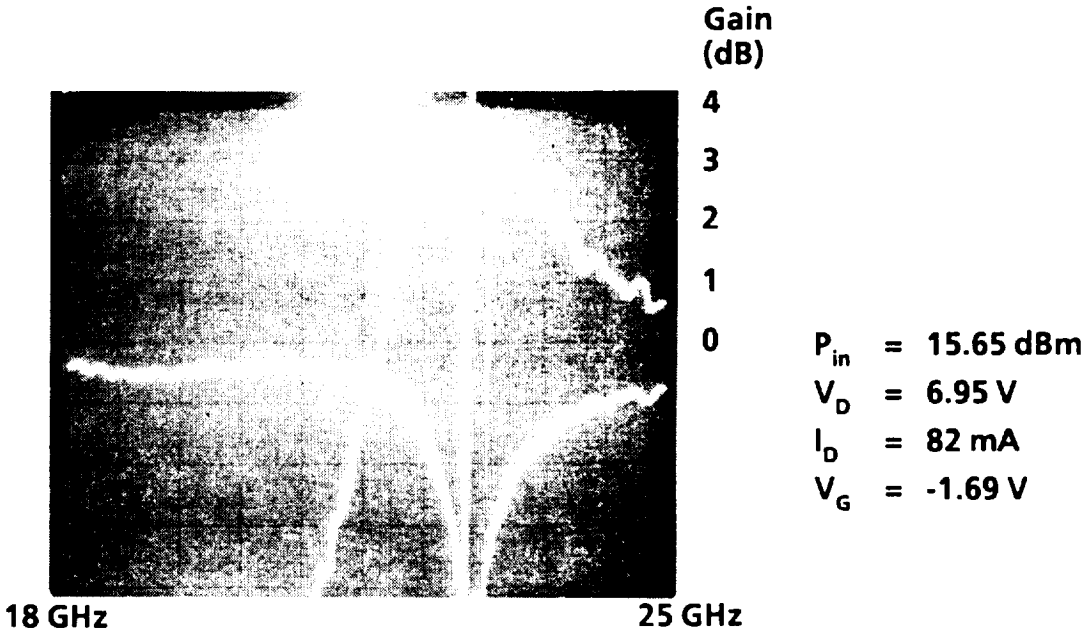


Figure 16.
Gain-frequency response of a one-stage amplifier with inductor to ground, with tuning.

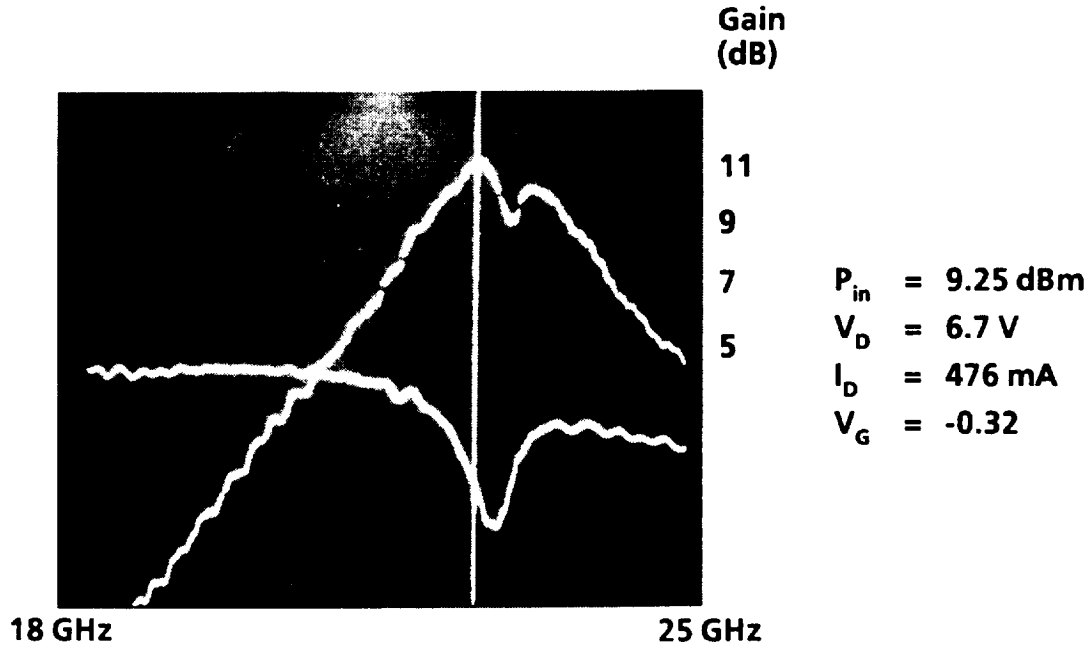


Figure 17.
Gain-frequency response of a two-stage amplifier with inductor to ground, with tuning.

This amplifier is tuned at 19 GHz and has very good performance at this frequency. It is capable of 800 mW output power with almost 15 dB gain. Figure 18 shows the amplifier gain-frequency response under these conditions. More work needs to be done in analyzing the performance of these amplifiers.

The two-stage amplifier with capacitor to ground is already very good, but the corresponding three-stage amplifier does not have better performance. In addition, although the three-stage amplifier with inductor to ground has fairly good gain and power, the frequency is too low.

The effort on the 23 GHz amplifier was discontinued in order to emphasize the 32.5 GHz amplifier.

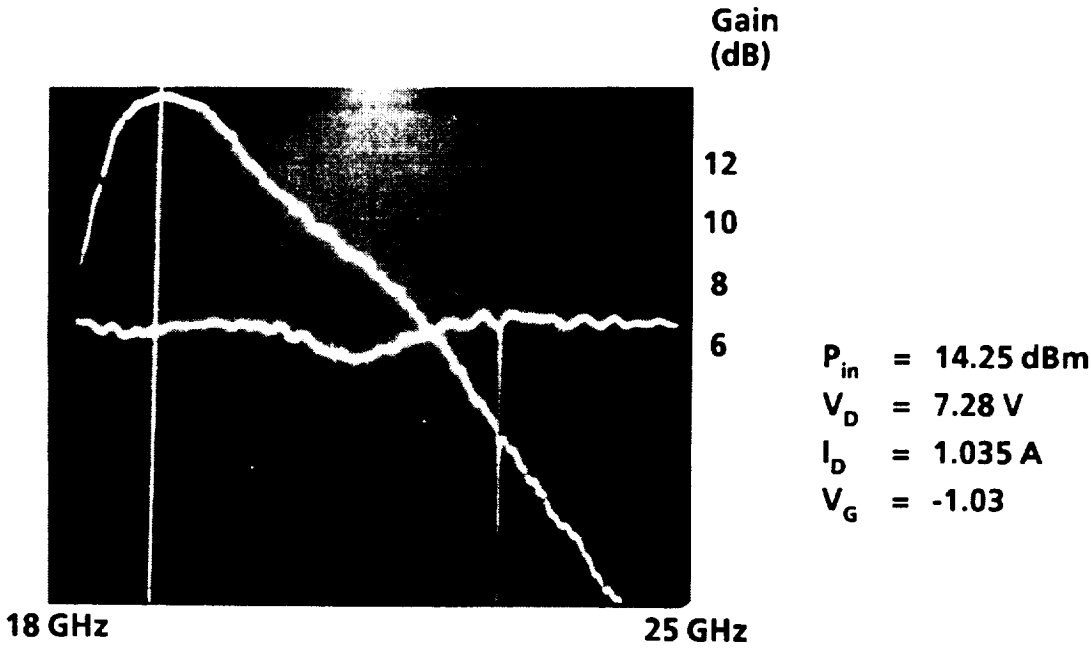


Figure 18.
Gain-frequency response of three-stage amplifier with inductor to ground, with tuning.

SECTION III
32.5 GHz AMPLIFIER DESIGN AND FABRICATION

The block diagrams for the 250 mW and 100 mW amplifiers are shown in Figure 19. In order to facilitate the evaluation of input, output, and interstage matching networks, one- and two-stage submodules were also designed and laid out.

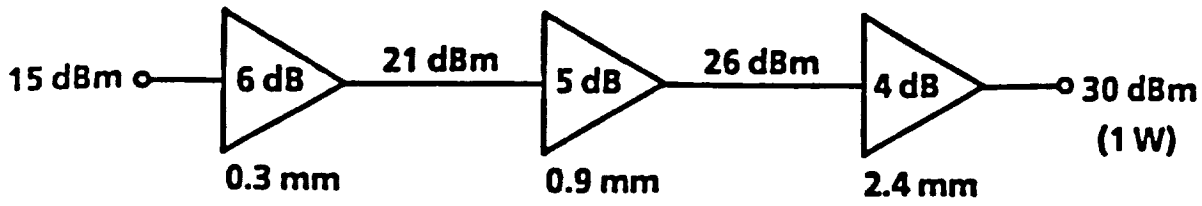
A. INITIAL DESIGN USING MESFET MATERIAL

Photographs of the six modules and submodules are shown in Figure 20. We used VPE MESFET material for the first lot. The gate lengths were, respectively, 0.5, 0.4, and 0.35 μm. On all wafers, the pinchoff voltage was ~2.5 V, which is too low for optimum performance. Table 2 summarizes the performance of the chips with 0.35 μm gates.

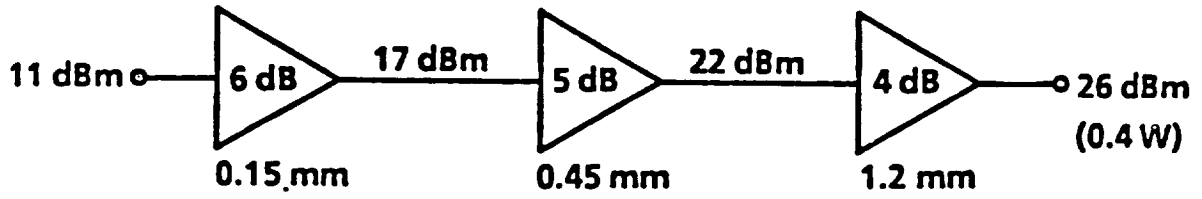
Table 2.
Performance of Chips With 0.35 μm Gates

Amplifier	Gain (dB)	Frequency (GHz)	Outside Tuning? (Yes or No)
Nominal 100 mW design			
Stage 1 submodule	3.5	34 to 37	No
	4	34	Yes
Stage 1-2 submodule	4	39 to 42	No
	5.5	34 to 37	Yes
Stage 1-2-3 module	5	43	No
	7	43	Yes
Nominal 250 mW design			
Stage 1 submodule	3	32.5	No
	4	32.5	Yes
Stage 1-2 submodule	6	31 to 33	No
Stage 1-2-3 module	10	32.5	No

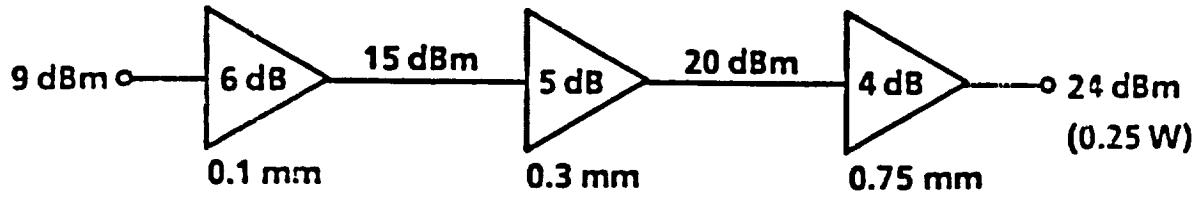
Three MBE wafers were processed in the next lot with gate lengths of 0.3 μm, 0.3 μm, and 0.4 μm, respectively. They also had the desired pinchoff voltage (3.5 to 4 V). The dc yield of the nominal 250 mW amplifier and the submodules is summarized in Table 3. The performance of the chip was similar to that of the amplifier fabricated on VPE slices, with a gain of 1 to 2 dB higher. Much better performance had been expected, since the device characteristics (saturation current, pinchoff voltage, and transconductance) were excellent.



(a) 23 GHz Band

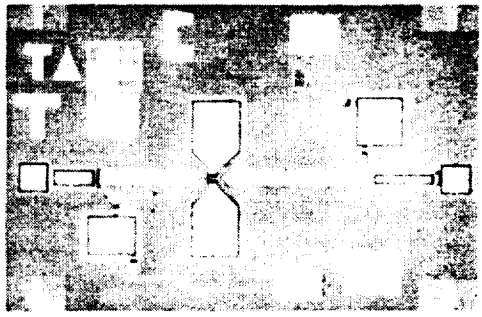


(b) 29 GHz Band

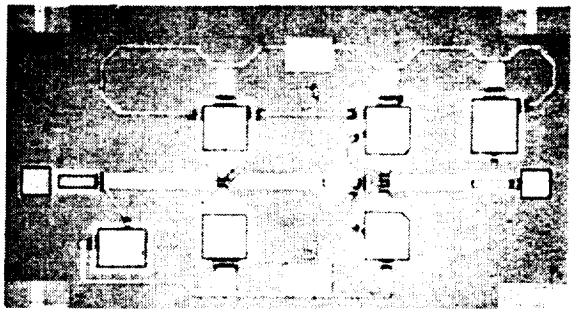


(c) 32.5 GHz Band

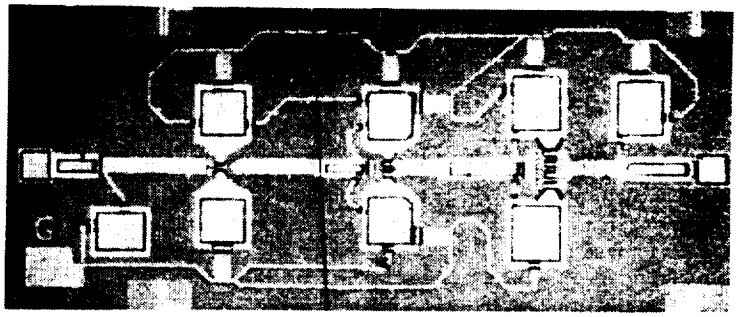
Figure 19. Block diagram of the amplifiers.



(a) 100 mW Stage 1 Submodule

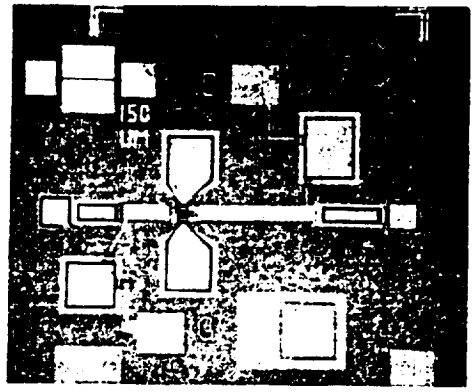


(b) 100 mW Stage 1-2 Submodule

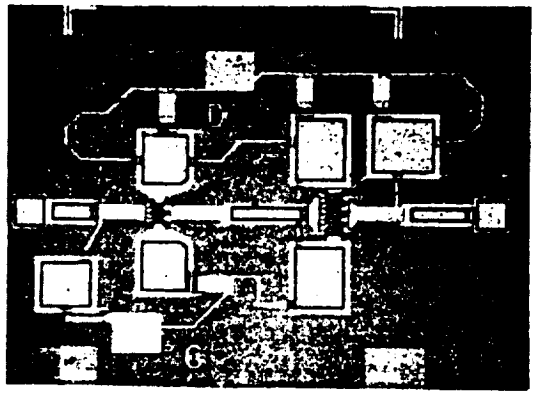


(c) 100 mW Module

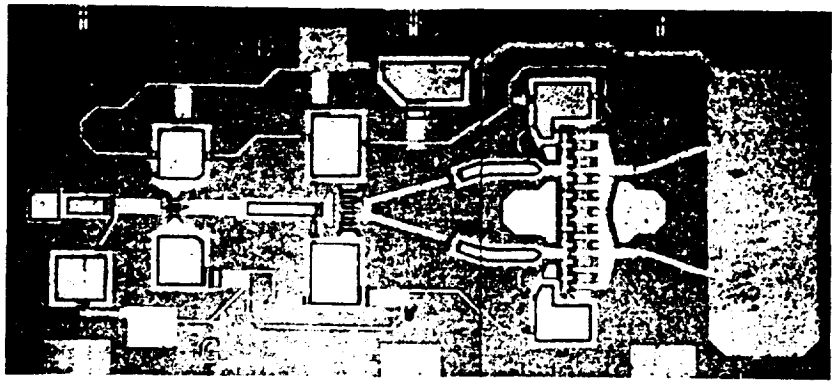
Figure 20. 32.5 GHz amplifier. (a) 100 mW stage 1 submodule, (b) 100 mW stage 1-2 submodule, (c) 100 mW module, (d) 250 mW stage 1 submodule, (e) 250 mW stage 1-2 submodule, (f) 250 mW module.



(d) 250 mW Stage 1 Submodule



(e) 250 mW Stage 1-2 Submodule



(f) 250 mW Module

Figure 20. (Continued)

Table 3.
DC Yield of Nominal 250 mW Amplifier and Submodules

Slice	Three-Stage Module Yield (%)	Two-Stage Submodule Yield (%)	One-Stage Submodule Yield (%)
MBE 744	33	31	61
MBE 775	45	45	80
MBE 764	20	33	33

To isolate the problem, a 100 μm device was separated from a single-stage amplifier and tested. Its performance was very good with a small signal gain of 8.5 dB at 35 GHz. When tuned for maximum output power, the device was capable of a power density of more than 0.4 W/mm with 4 dB gain. To check the circuit loss, the following experiments were conducted. The FET and the two microstrip lines shunted to ground were scratched off the chip, and wires were bonded across the input and output microstrip lines. The measured loss was 0.5 dB. This showed that the loss of the two bypass capacitors and the microstrip line was small. With the FET scratched off and wires bonded across the input and output microstrip lines, the output shunt line was scribed off, and tuning was performed. The loss was less than 1 dB. The same experiment performed with the input line scribed off produced the same result. This showed that the input and output matching circuits (shunt lines and bypass capacitors) did not have excessive loss.

Modifications were done on the one-stage and two-stage amplifiers (submodules of the 32.5 GHz, 250 mW amplifier). On the one-stage (100 μm FET) amplifier, the length of the input series transmission line was effectively decreased by scratching the shunt transmission line and replacing it with a bond wire closer to the FET. On the output, the series transmission line was increased by scratching it and introducing a bond wire. After these modifications, the small-signal gain was 7 to 8 dB (Figure 21), which corresponded to the results obtained with a discrete device reported previously.

The two-stage amplifier was also modified (using carefully bonded wires), and produced a small-signal gain as high as 15 dB. The gain curve is shown in Figure 22. These modifications show that the FETs have a higher input capacitance than that predicted by the model, while the equivalent output shunt capacitance and resistances are lower.

The 150-300-800 μm amplifier had 12 dB gain without tuning (Figure 23). By appropriate tuning of the input and interstage matching network (with bond wires), we obtained 18 dB gain with 0 dBm input power. The gain curve is shown in Figure 24.

The 50 μm single-stage amplifier was internally modified using bond wires: the input shunt inductor was moved closer to the input, and the output shunt inductor was moved away from the

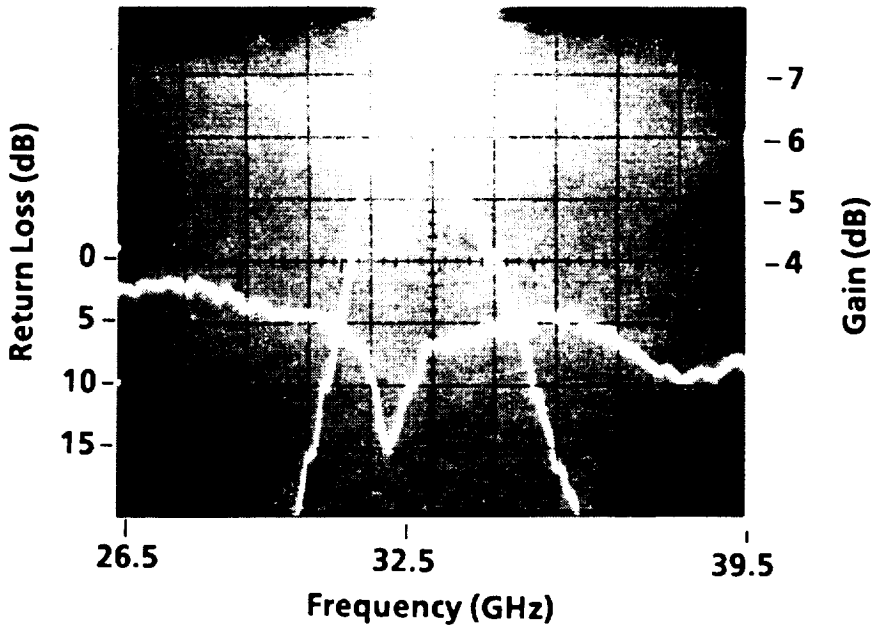


Figure 21. Gain (upper trace) and return loss (lower trace) of a modified one-stage amplifier (does not include 0.8 dB fixture loss).

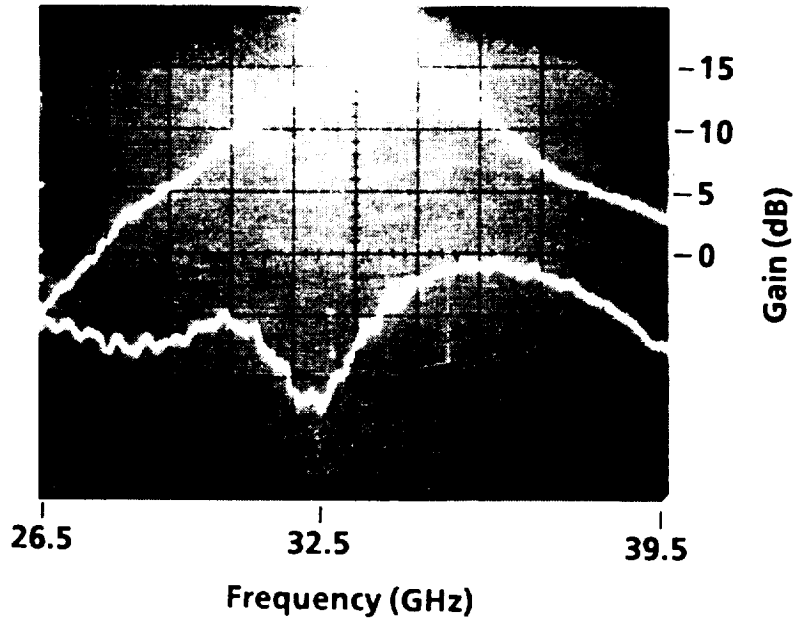


Figure 22. Gain (upper trace) and return loss (lower trace) of a modified two-stage amplifier (does not include 0.8 dB fixture loss).

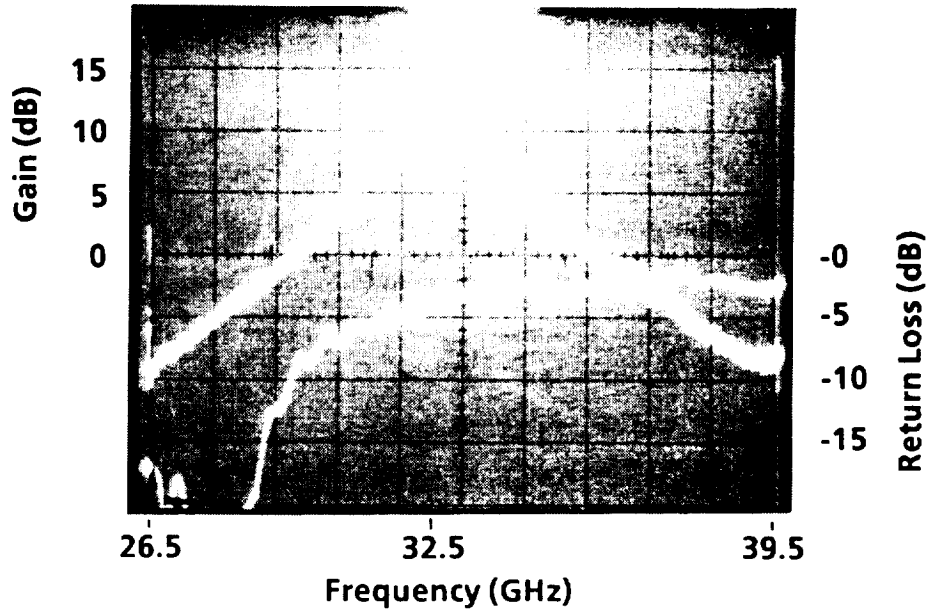


Figure 23. Gain curve of the 150-300-800 μm amplifier with no modifications.

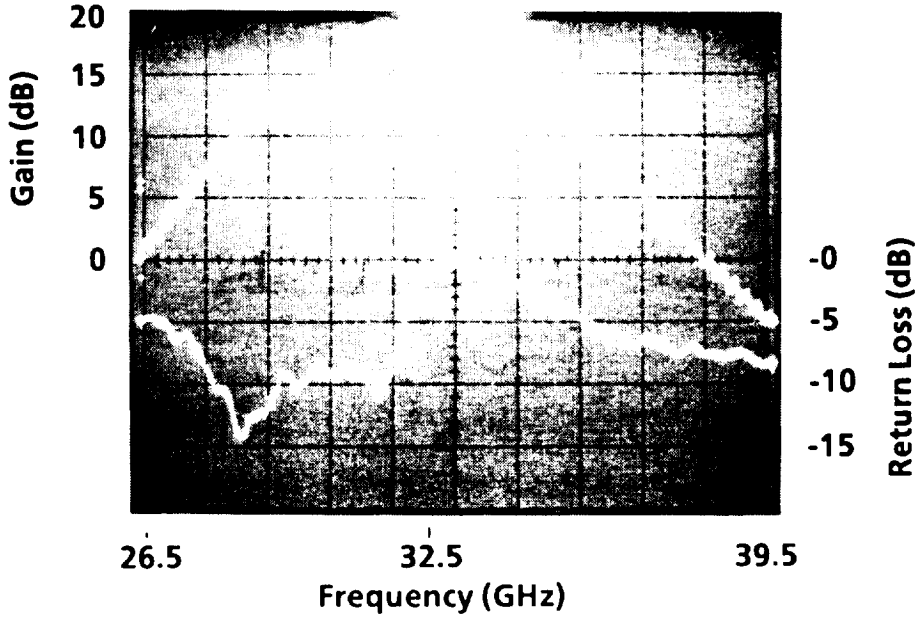


Figure 24. Gain curve of the 150-300-800 μm amplifier with modifications.

FET drain. These modifications produced a gain of 6 dB. This means that the input capacitance of the FET was higher than that modeled, and the output capacitance C_{ds} was smaller than that modeled.

The gain of the two-stage amplifier was 11 to 12 dB with 0 dBm input power (Figure 25) when chip tuning was performed on the input, the interstage series transmission line was made longer, and the output shunt inductor was moved away from the FET drain.

The gain of the three-stage amplifier was 15 dB with –10 dB input power (Figure 26) after the lengths of the 1-2 and 2-3 interstage transmission lines were increased and the shunt inductor on the output of the third stage was moved away from the drain. These modifications were implemented in a new inductor mask, and wafers were processed. The performance of these amplifiers was much better than that of the previous chips.

Extensive testing has been done with the large (250 mW) module and submodules. The results are summarized below:

One-Stage Amplifier

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–5.5	9.5	11
4.5	6.2	
9.5	4.1	
11.5		4.1

Figure 27 shows the gain-frequency response of a first-stage amplifier for input powers of –5.5, 4.5, and 9.5 dBm. A 1 dB gain should be added, because the fixture loss has not been taken into account. The one-stage amplifier works very well. The gain is centered around 34 GHz and can be lowered to 32.5 GHz with slight input tuning. Small-signal gains as high as 11 dB can be obtained with input tuning. A maximum power density of 0.36 W/mm with 4.1 dB gain at 34 GHz is obtained with 19.5% PAE.

Two-Stage Amplifier

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
0	16	—
4.5	12.3	—
9.5	8	

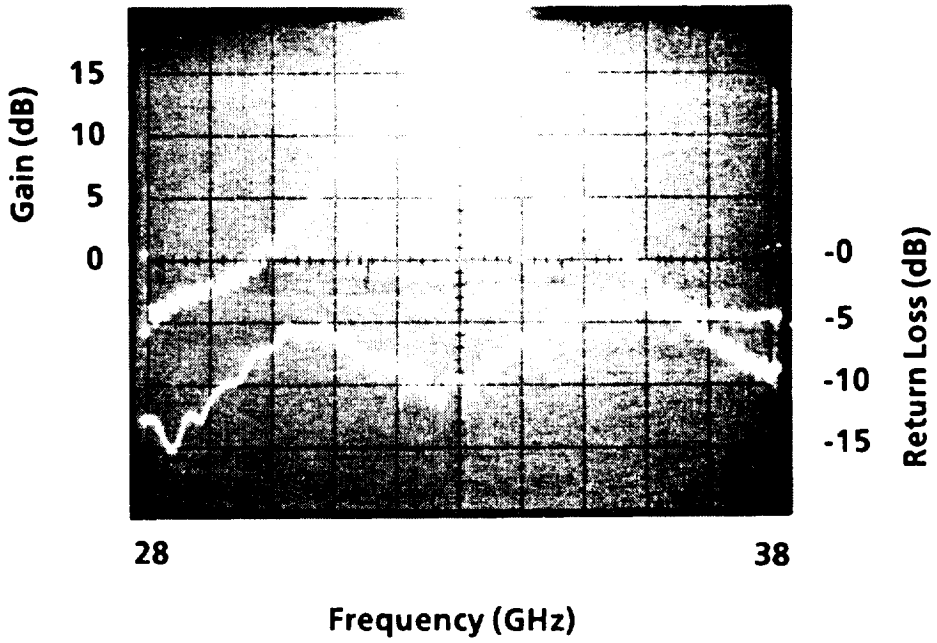


Figure 25. Gain curve of the 50-100 μm amplifier with modifications.

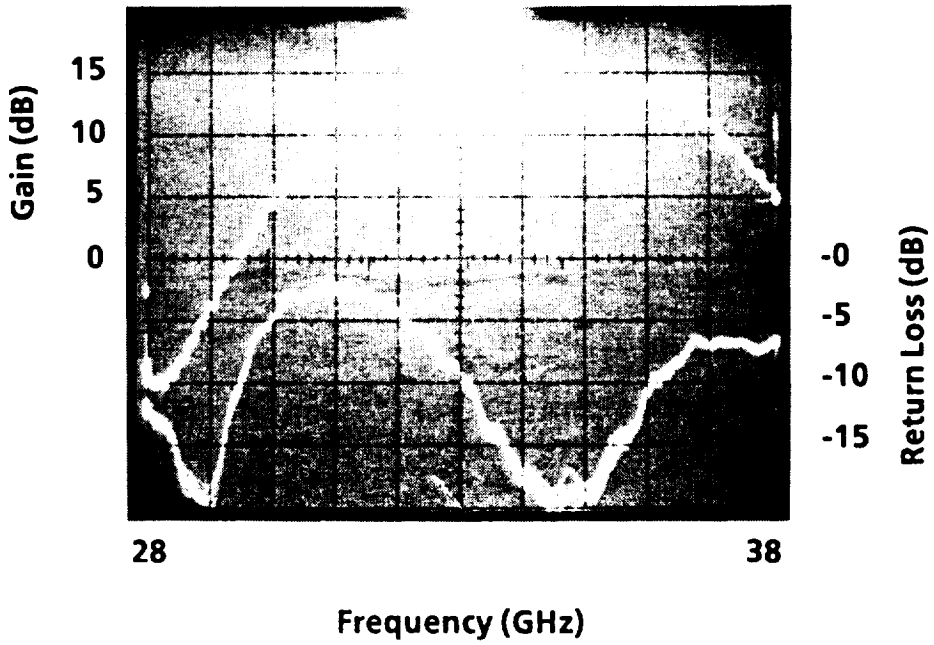
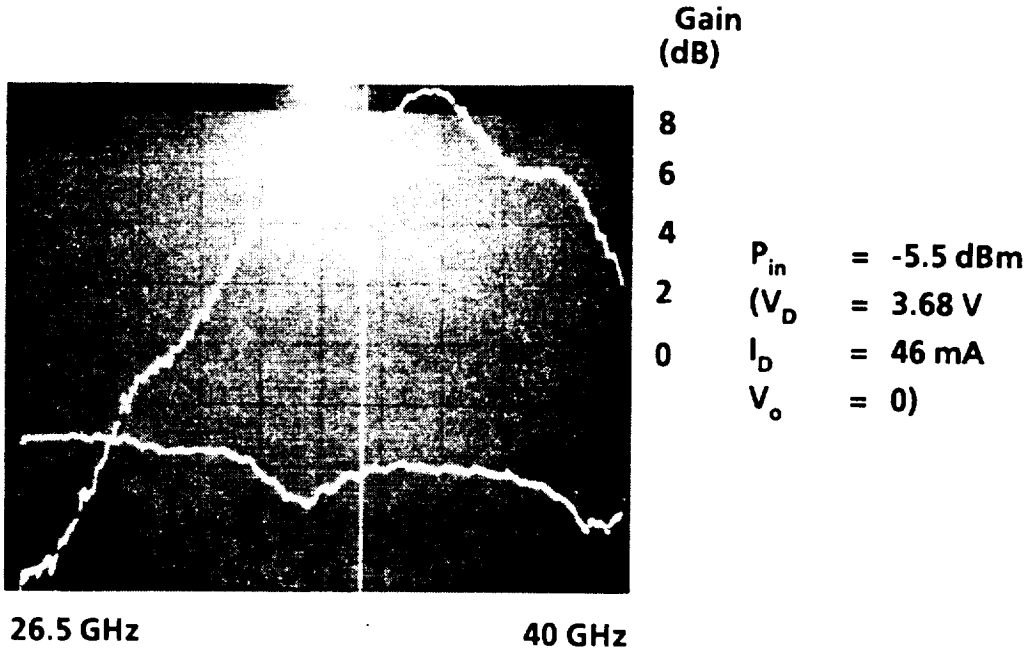
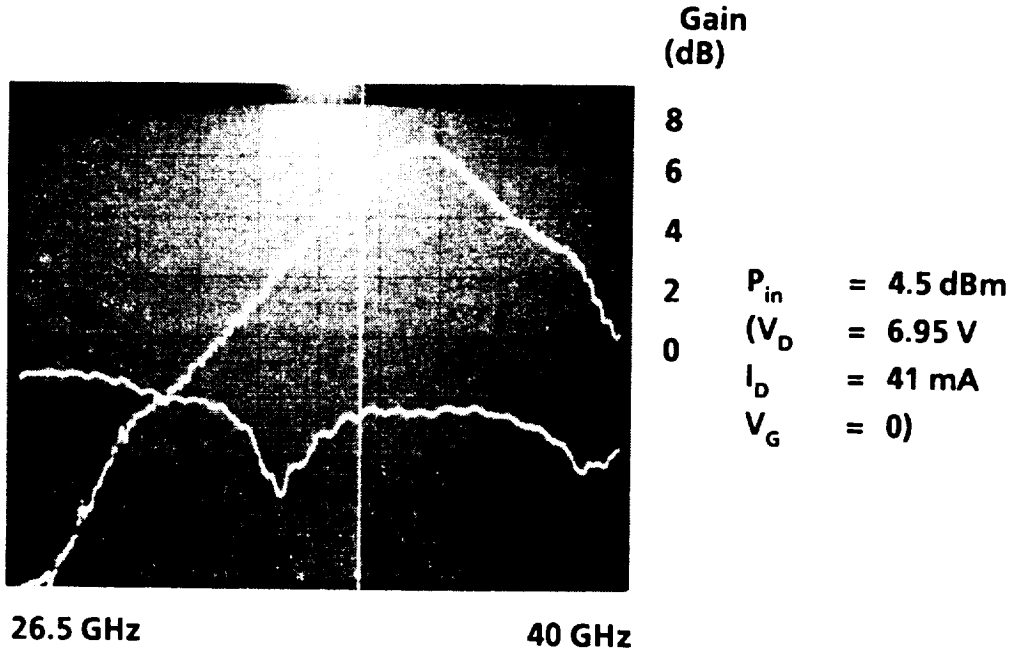


Figure 26. Gain curve of the 50-100-250 μm amplifier with modifications.



(a)



(b)

Figure 27. Gain-frequency response of a one-stage amplifier for input powers of (a) –5.5 dBm, (b) 4.5 dBm, (c) 9.5 dBm.

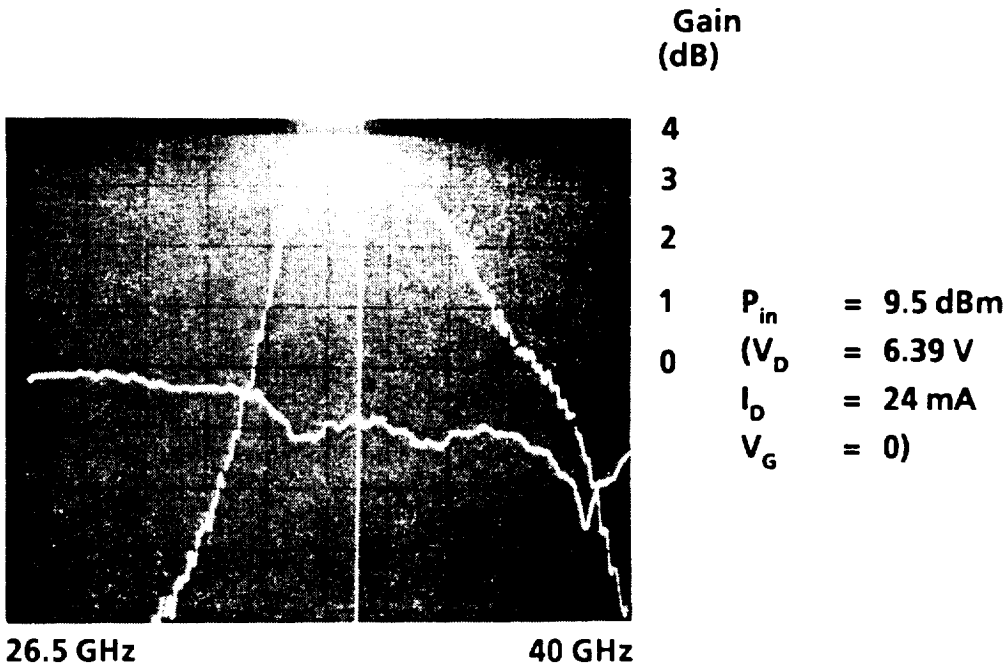


Figure 27. (Continued)

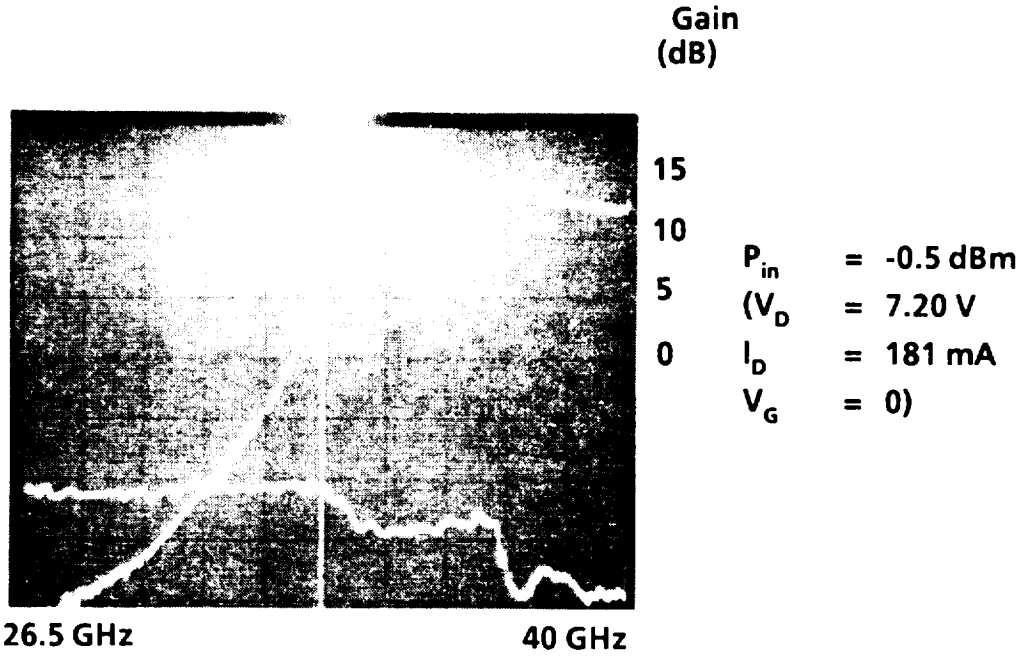
Figure 28 shows the gain-frequency response of a two-stage amplifier for input powers of –0.5, 4.5, and 9.5 dBm (fixture loss of 1 dB not taken into account). The two-stage amplifier also has an excellent small-signal gain of 16 dB. It is tuned a little high (37 GHz), but this frequency can be lowered with input and output tuning.

The maximum output power was 17.5 dBm with 8 dB gain, corresponding to a power density of 0.19 W/mm. This was too low and showed that the last stage was tuned for small-signal gain, not for power gain. Another indication was that the best performance was obtained with 0 V on the gate; power tuning usually requires –1 to –1.5 V on the gate.

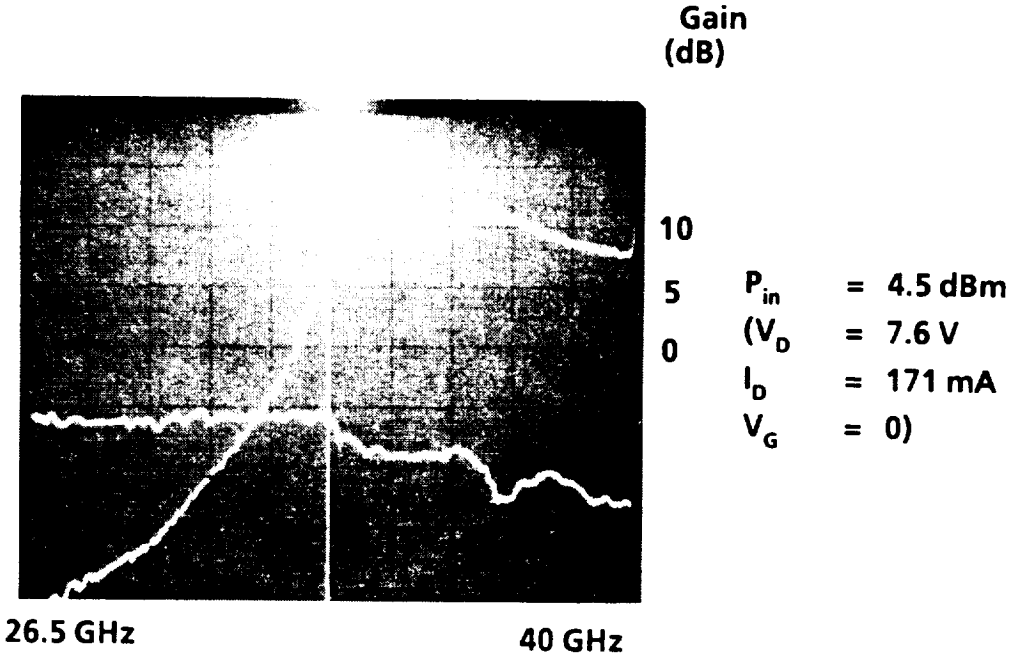
Three-Stage Amplifier

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
5.5	21	22
4.5	15	—
9.5	10.5	—

Figure 29 shows the gain-frequency response of a three-stage amplifier for input powers of –5.5, 4.5, and 9.5 dBm (fixture loss of 1 dB not taken into account). The three-stage amplifier was also tuned for small-signal gain. With no tuning, up to 22 dB gain at 34 GHz could be obtained. A maximum power of about 110 mW could be achieved. This was too low. We sawed an 800 μm device with its matching circuit (the last stage of the three-stage amplifier) and tested it around



(a)



(b)

Figure 28. Gain-frequency response of a two-stage amplifier for input powers of (a) –0.5 dBm, (b) 4.5 dBm, (c) 9.5 dBm.

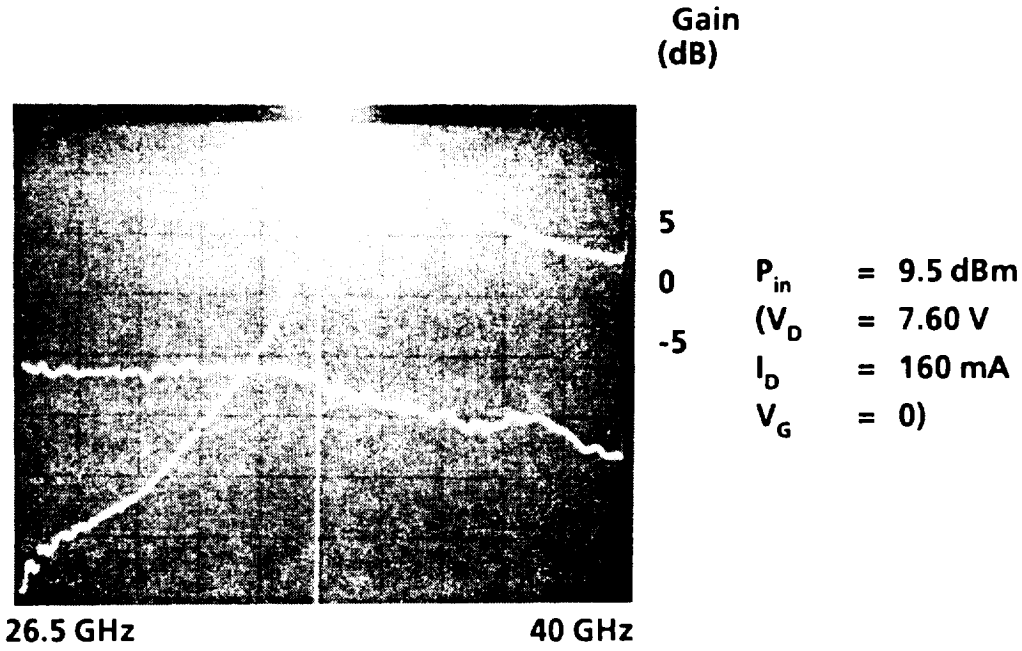
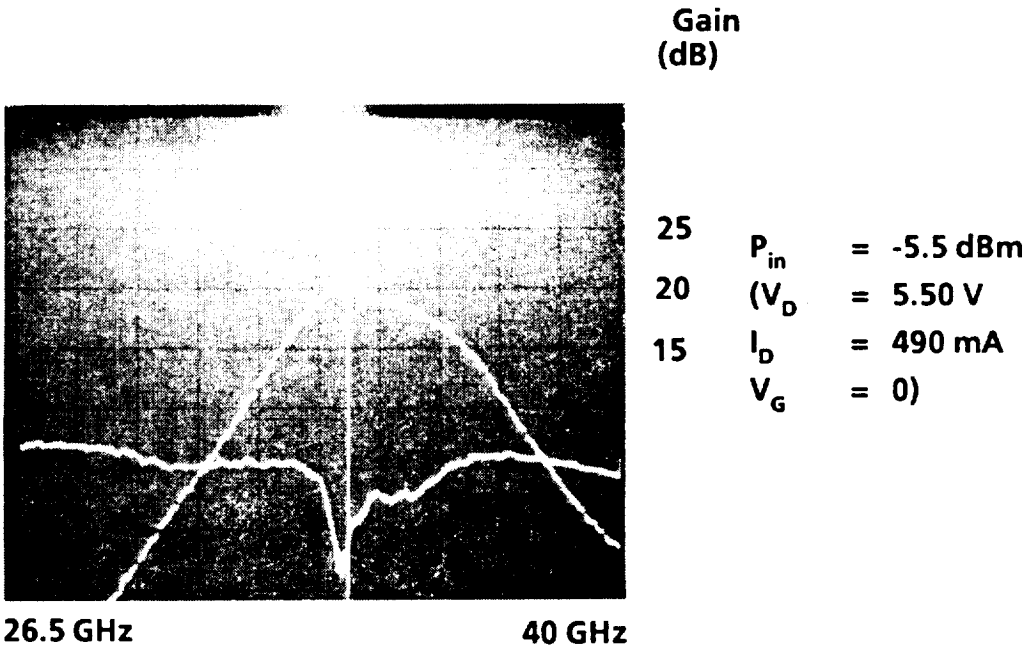
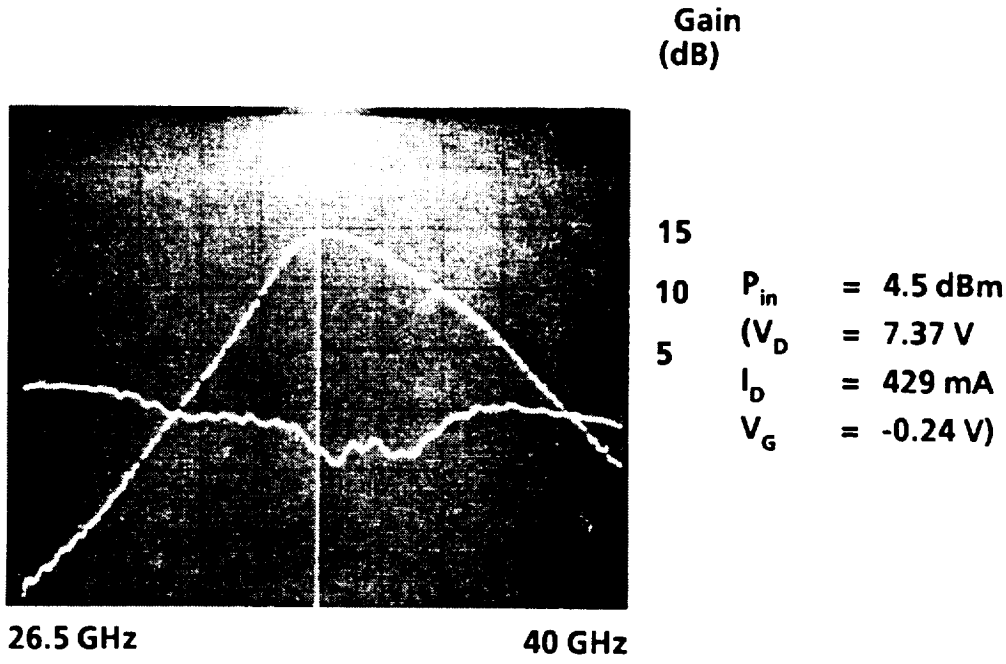


Figure 28. (Continued)



(a)

Figure 29. Gain-frequency response of a three-stage amplifier for input powers of (a) –5.5 dBm, (b) 4.5 dBm, (c) 9.5 dBm.



(b)

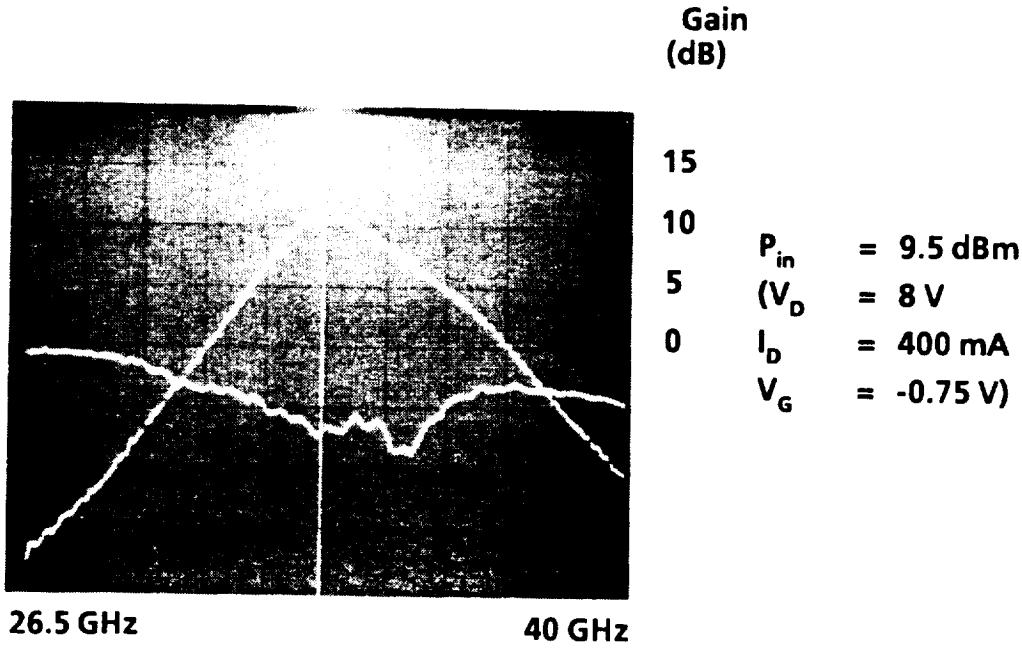


Figure 29. (Continued)

30 GHz. Small-signal gain was low, and not much power could be obtained. This indicated that the structure and layout of the FET were not adequate.

Preliminary testing was done on the two- and three-stage small (100 mW) amplifiers. They were tuned too high—around 39 GHz.

Two-Stage Amplifier

Input Power (dBm)	Gain (dB) (No Tuning)	Gain (dB) (Tuned)
–10.5	13	17
–0.5	10	—
4.5	—	8

Figure 30 shows the gain-frequency response of a two-stage amplifier for input powers of –10.5, –0.5, and 4.5 dBm (a fixture loss of 1 dB not taken into account). With input and output tuning, the two-stage amplifier had a small-signal gain of up to 17 dB at 36 GHz. A three-stage amplifier was capable of 22 dB small-signal gain (Figure 31).

B. REVISED DESIGN WITH MBE HIGHLY DOPED MESFET MATERIAL

Three wafers with highly doped material (8×10^{17} cm^{-3}) were processed next. The dc characteristics were very good, and transconductances were 200 to 240 mS/mm. Testing on the one-stage (100 μm), two-stage (100-300 μm) and three-stage (50-100-250 μm) gave the following results.

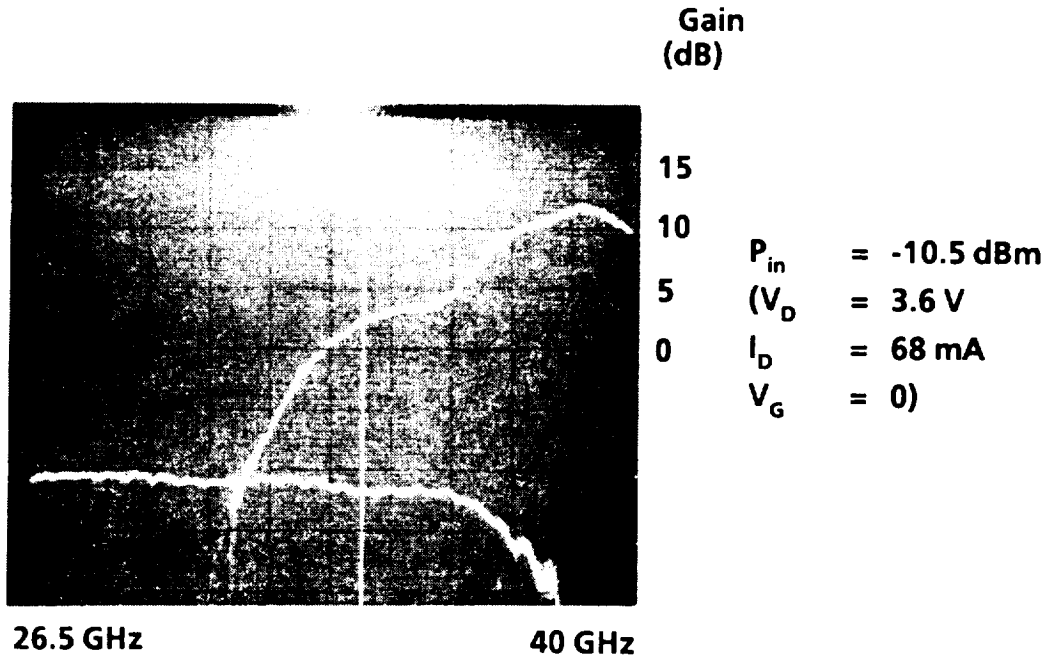
1. One-Stage Amplifier (100 μm)

When biased for small-signal gain, the amplifier has more than 10 dB gain with input and output tuning. When tuned for power, the amplifier is capable of 47 mW output power with 5.2 dB gain and 23% PAE at 33 GHz. The 1 dB bandwidth is 3 GHz. This is a record PAE for an MMIC amplifier at this frequency. Figure 32 shows the output power as a function of frequency for an 11.5 dBm input power for maximum efficiency.

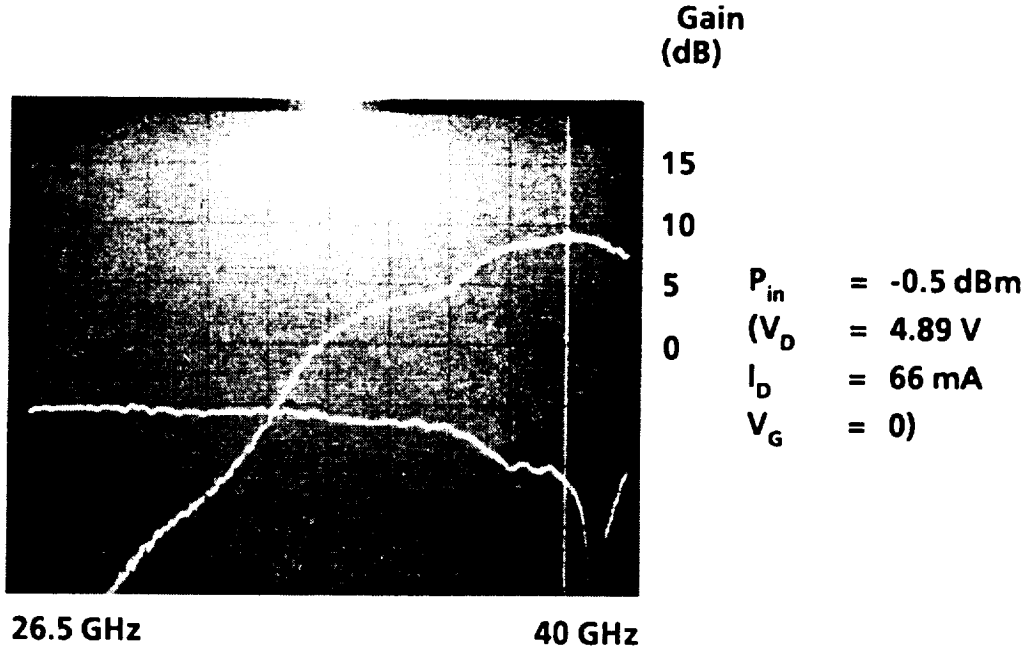
2. Two-Stage Amplifier (100-300 μm)

With no outside tuning, the amplifier has up to 17 dB small-signal gain at around 37 GHz. Figure 33 shows the corresponding gain-frequency response. When tuned for power, the amplifier achieves 120 mW output power with 8.8 dB gain and 15.6% PAE. The corresponding linear gain is 11.3 dB (Figure 34).

To demonstrate efficiency, a hybrid amplifier was assembled using a very good 75 μm discrete highly doped FET. Figure 35 shows the output power as a function of frequency for different input powers. Figure 36 is the corresponding gain compression curve at 32.5 GHz. The small



(a)



(b)

Figure 30. Gain-frequency response of a two-stage amplifier for input powers of (a) −10.5 dBm(no tuning), (b) −0.5 dBm (no tuning), and (c) 4.5 dBm (tuned on the output).

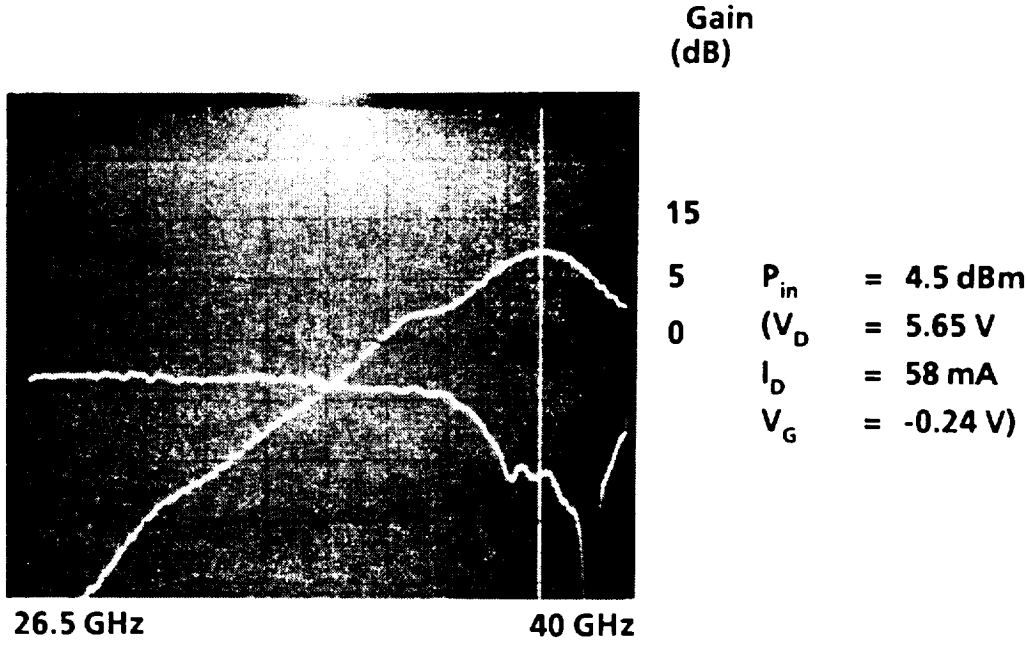


Figure 30. (Continued)

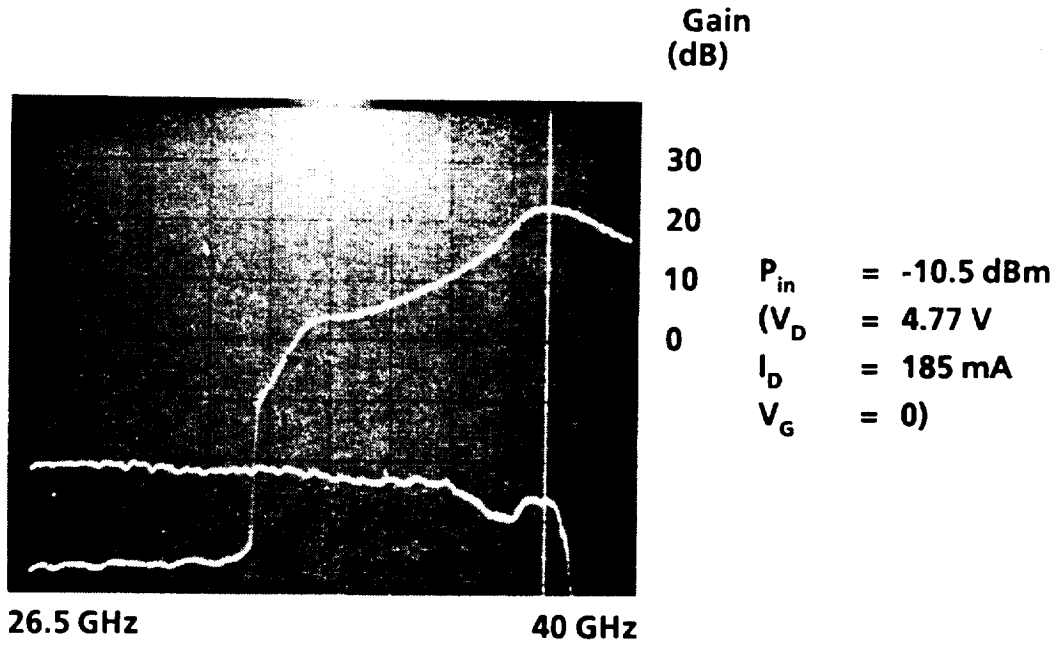


Figure 31. Gain-frequency response of a three-stage amplifier for an input power of −10.5 dBm.

V_D = 5.38 V
I_D = 26 mA
V_G = -1.34 V

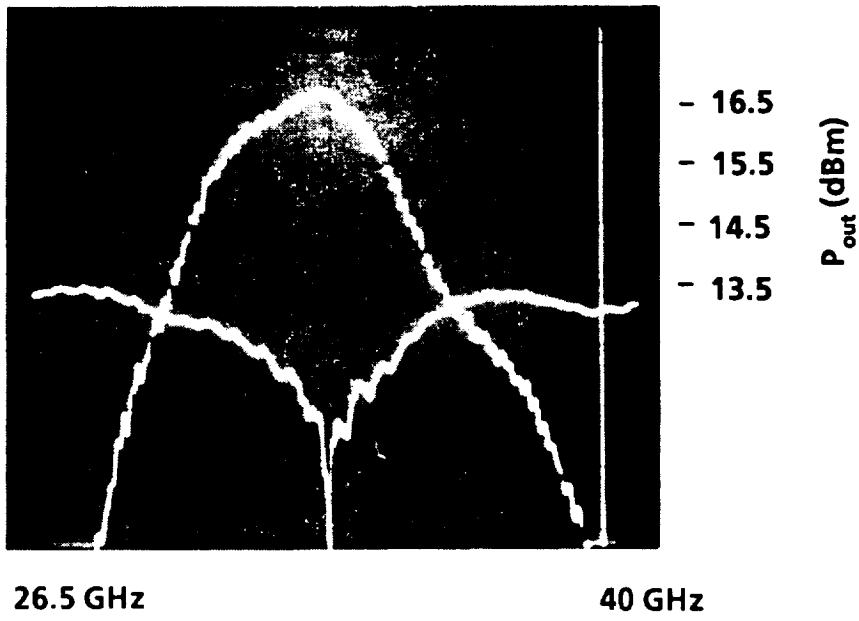


Figure 32. Output power as a function of frequency for a one-stage amplifier (100 μm) with P_{in} = 11.5 dBm.

V_D = 5.5 V
I_D = 169 mA
V_G = 0 V

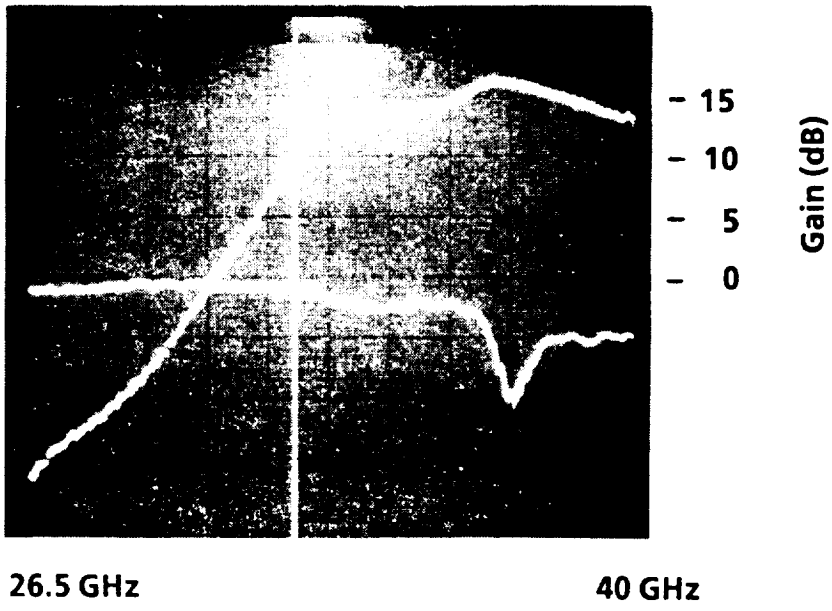


Figure 33. Gain-frequency response for a two-stage amplifier (100-300 μm)with an input power of –0.5 dBm.

V_D = 6.5 V
I_D = 103 mA
V_G = -1.13 V

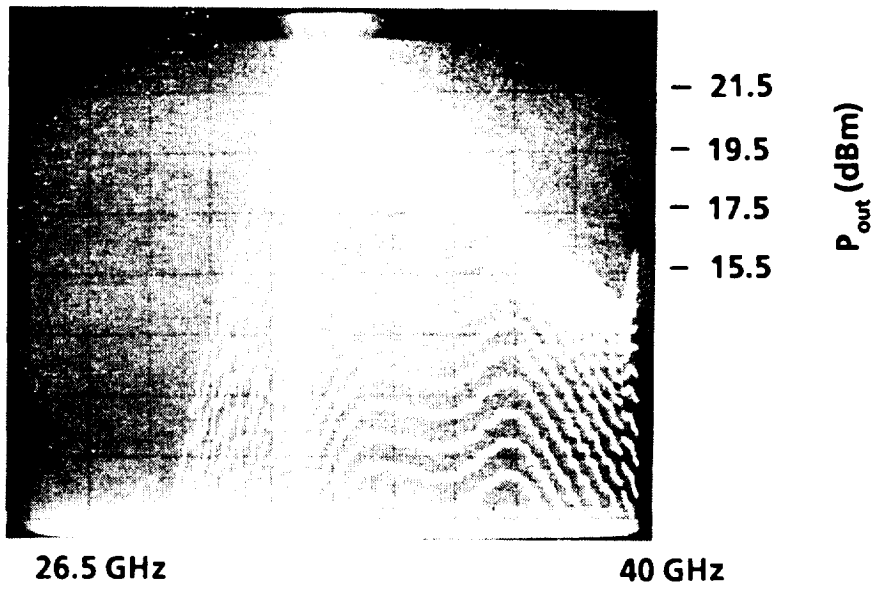


Figure 34. Output power as a function of frequency for a two-stage amplifier (100-300 μm).Lower trace, P_{in} = –4.5 dBm, spacing 1 dB.

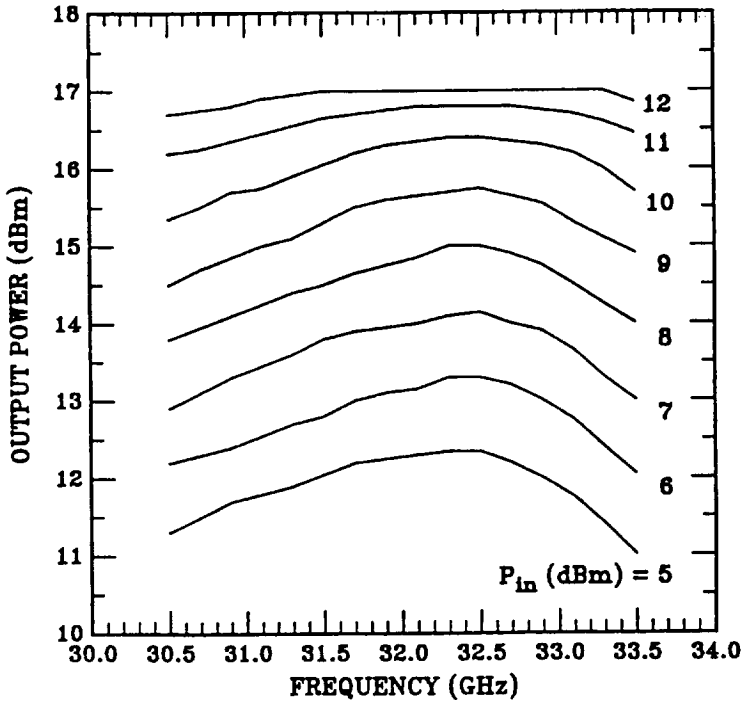


Figure 35. Frequency response of a 32.5 GHz, 75 μm hybrid amplifier.

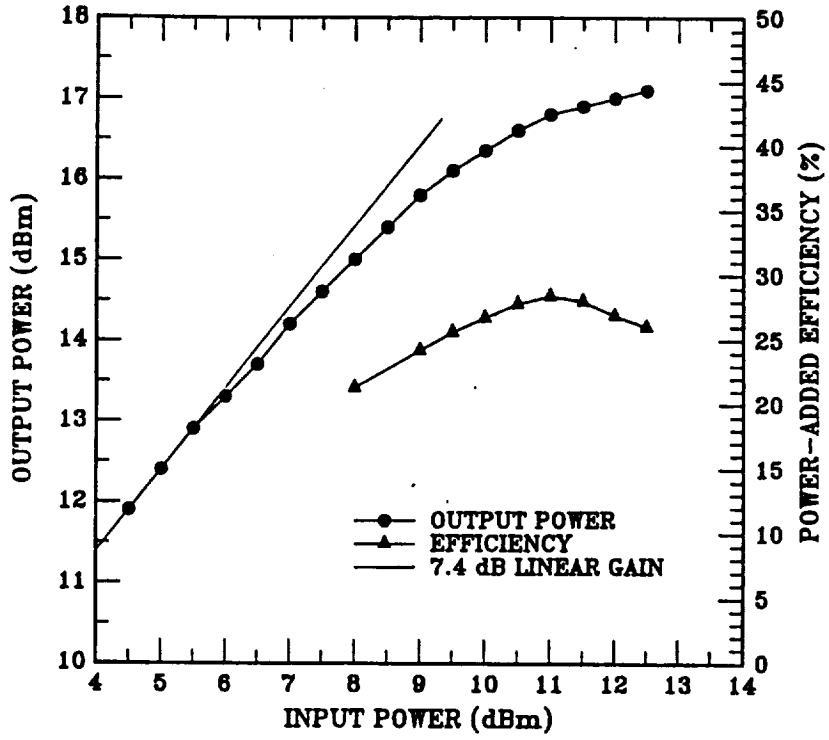


Figure 36. Gain compression curve of a 75 μm hybrid amplifier.

signal gain is 7.4 dB, and a maximum efficiency of 28% is achieved with 16.75 dBm (0.63 W/mm) and 5.75 dB gain.

3. Three-Stage Amplifier (50-100-250 μm)

A maximum small-signal gain of 26 dB was obtained with 4 V drain bias and 0 V gate bias. When biased for large-signal operation (V_D = 4.7 V, V_G = –0.5 V), the amplifier was capable of generating 112 mW output power with 16 dB gain and 21.6% PAE at 34 GHz (linear gain of 21.2 dB). These results were state of the art when they were achieved. They were presented at the 1988 GaAs IC Symposium.

C. REVISED DESIGN ON DOPED-CHANNEL HEMT MATERIAL

Much improved performances were achieved by using the "doped-channel HEMT." This material allows very high current density (0.8 to 0.9 A/mm) with very high transconductance (500 to 700 mS/mm) and moderate breakdown voltage (7 to 9 V). Again, new state-of-the-art results were achieved with the one-, two-, and three-stage amplifiers. A record 40% efficiency was obtained with the single-stage 100 μm amplifier with 63 mW and 65 dB gain. Table 4 summarizes the performance of the amplifiers. The 50-100-250 μm amplifier achieved 180 mW output power with

23 dB gain and 30.3% efficiency. This represented a record efficiency for a multistage MMIC at this frequency.

Table 4.
Amplifier Performances

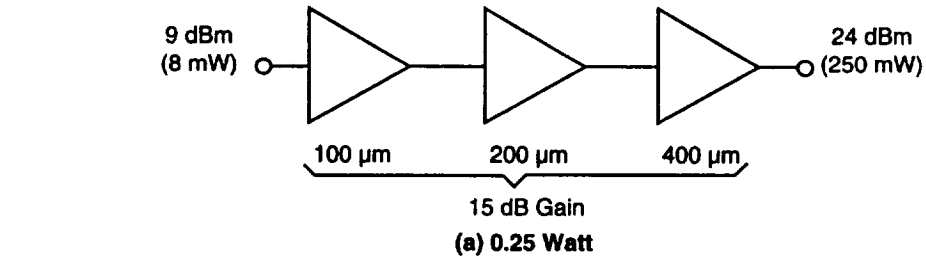
No. Stages	Gatewidth (μm)	Frequency (GHz)	Power (mW)	Gain (dB)	Efficiency (%)
1	100	32	91 (0.91 W/mm)	5.1	36.7
			63 (0.63 W/mm)	6.5	40
2	500-100	32	90 (0.9 W/mm)	14	25.9
			72 (0.7 W/mm)	13	31.3
3	500-100-250	31	180 (0.76 W/mm)	233	30.3
1	800	31	720 (0.90 W/mm)	4.2	25
3	100-300-800	29	390	16	25

SECTION IV
32.5 GHz HIGH-EFFICIENCY 250 mW AND 1 W POWER AMPLIFIER DEVELOPMENT

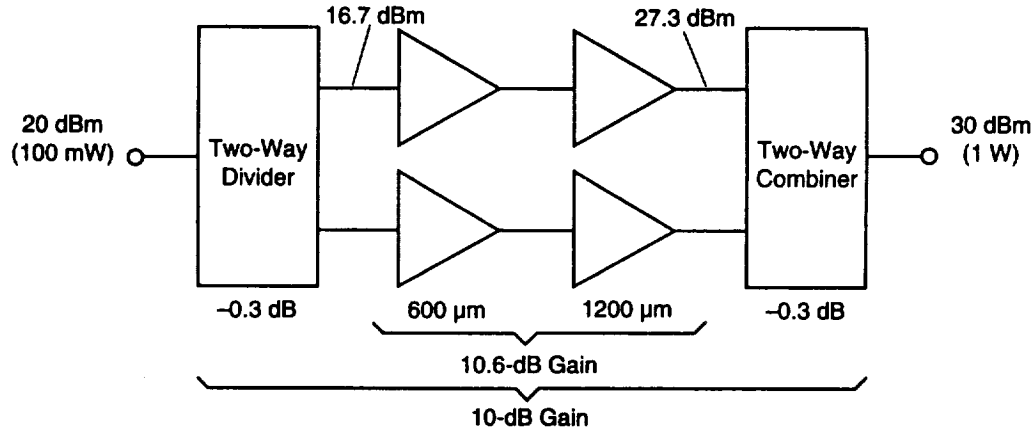
The objective of this program modification was to demonstrate the feasibility of 32.5 GHz amplifiers with even higher efficiency and power. Specifically, goals for the amplifiers were:

- 250 mW with ≥15 dB gain and ≥50% PAE
- 1 W with ≥ 10 dB gain and ≥35% PAE

The block diagrams of the amplifiers are shown in Figure 37. The 250 mW amplifier has three stages with 100, 200, and 400 μm gatewidth. The 1 W amplifier combines 2 two-stage 600-1200 μm amplifiers. Figure 38(a) is the schematic circuit diagram of the three-stage 100-200-400 μm



(a) 0.25 Watt



Amplifier Type	Output Power (W)	Gain (dB)	Drain Voltage (V)	Drain Current (A)	DC Power (W)	Power-Added Efficiency (%)
600-μm/1200-μm	0.537	10.6	7	0.183	1.28	38
2× (600-μm/1200-μm)	1.0	10	7	0.366	2.56	35

(b) 1 Watt

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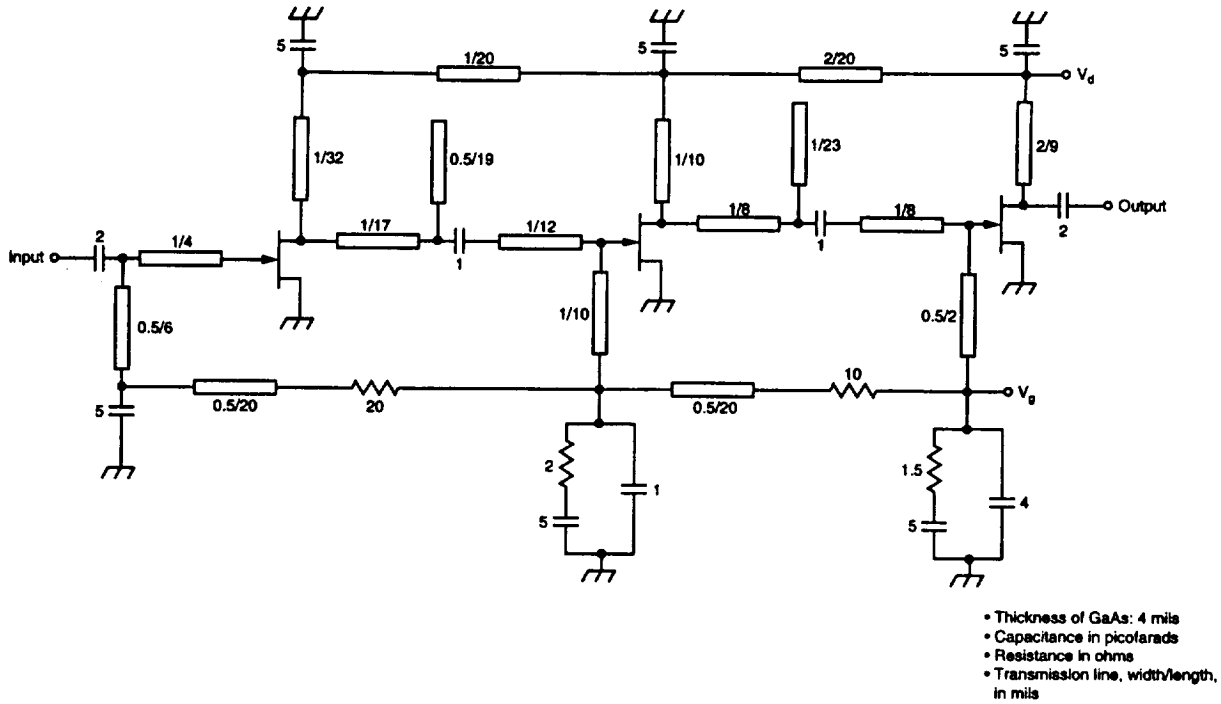
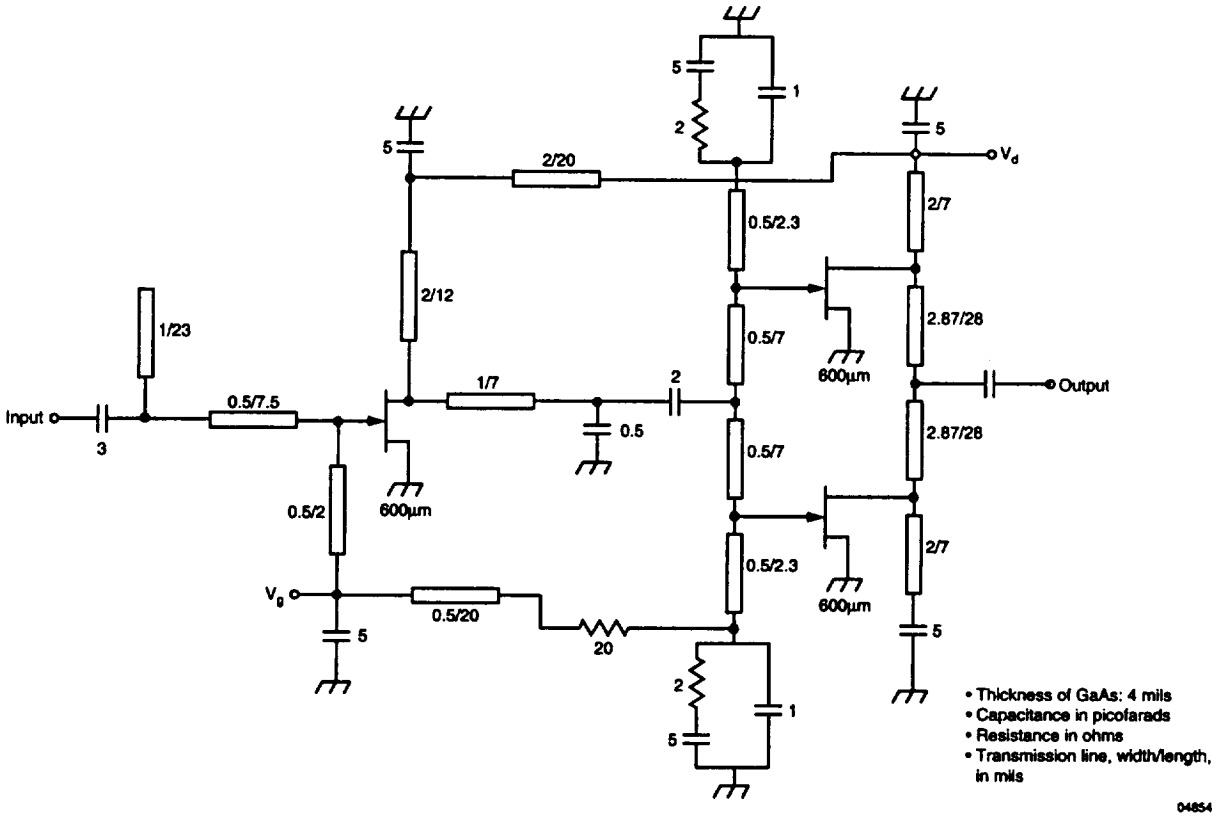
Figure 37. Block diagram of proposed amplifiers.



(a) Three-Stage 100-μm/200-μm/400-μm Amplifier



(b) Two-Stage 600-μm/1200-μm Amplifier

Figure 38. Amplifier schematic circuit diagrams.

amplifier. Figure 38(b) shows the two-stage 600-1200 μm circuit. The dimensions of the transmission lines, values of thin-film resistors, and matching/dc blocking MIM capacitors are also given. Provisions for out-of-band stabilization consist of RC filter networks on most of the gate bias circuits as shown. These filter networks are designed to provide resistive termination at out-of-band frequencies (primarily at lower frequencies where the device stability factor, k, is considerably less than unity). This network will have little or no effect on the amplifier in-band performance. Both amplifiers are provided with input and outpt dc blocking capacitors to facilitate testing and integration. Monolithic two-way combining of two 600-1200 μm amplifiers (with an output power goal of 1 W) are also included in the mask. Coplanar input and output are provided on each of the amplifiers to allow for RF on-wafer probing using CASCADE probes. Discrete devices of various sizes (gatewidths) are also included to facilitate device characterizations.

Figure 39 shows photographs of the three-stage 100-200-600 μm amplifier, the two-stage 600-1200 μm amplifier, and the 1200-2400 μm amplifier.

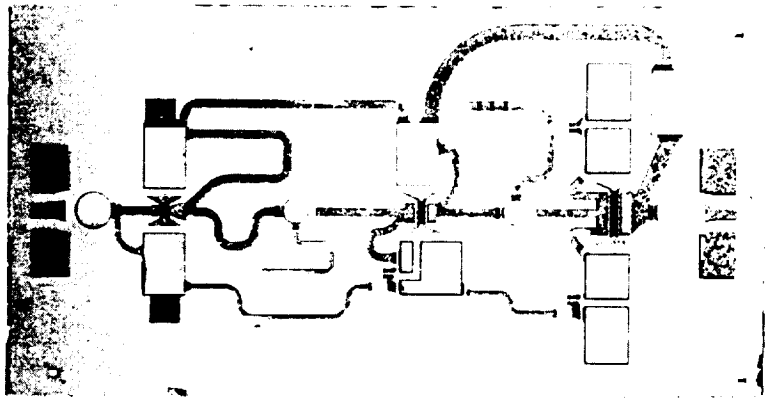
Initial fabrication was done on MBE doped-channel HEMT material where the InGaAs is 120 Å thick doped 2×10^{18} cm^{-3}, the top AlGaAs is 600 Å thick doped 2×10^{18} cm^{-3}, followed by a 300 Å GaAs n^+ cap layer. Table 5 summarizes performance at 31 GHz.

Table 5.
Performance Results for One Three-Stage Amplifier at 31 GHz

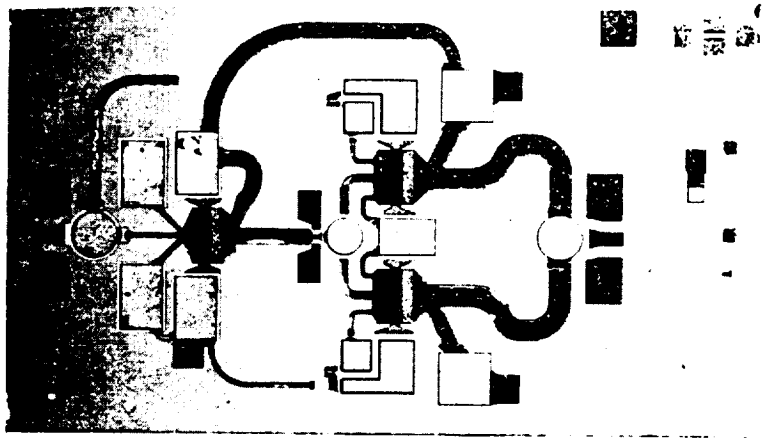
Power (mW)	Gain (dB)	PAE (%)	V_d (V)	I_d (mA)
200	18	36	4	140
240	18	34	4.5	164
280	17.5	31	5.0	180

At a drain voltage of 4 V, the PAE was 36% with 200 mW output and 18 dB gain. Increasing the drain voltage to 5 V produced an output power of 280 mW with 17.5 dB gain and 31% PAE. Note that a power density as high as 0.7 W/mm was obtained for the output stage (400 μm gatewidth). Figure 40 shows the performance of the three-stage amplifier over the 30.5 and 31.5 GHz frequency range.

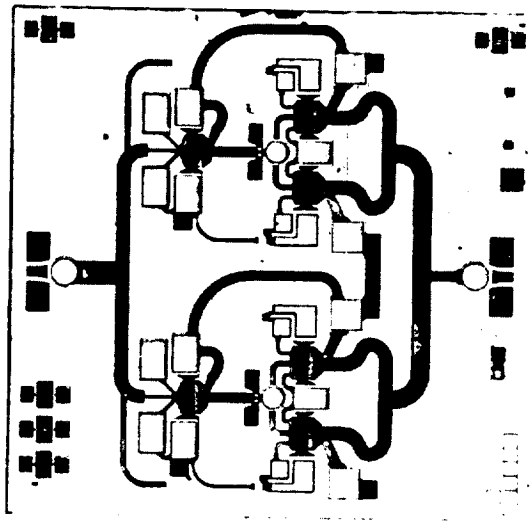
The two-stage 600-1200 μm amplifier had low gain and output power. The second stage (2 × 600 μm) was sawed off and characterized. Most of the interstage matching network and the original output matching network remained intact for analysis. One of the 2 × 600 μm chips had an output power of 560 mW with 4 dB gain and 31.3% PAE at 31 GHz. Another chip had an output power of 822 mW (V_d = 5 V) and a PAE of 28.3% (with 3.3 dB gain) at the same frequency. At a drain voltage of 5.62 V, a record output power of 900 mW (with 3.2 dB gain) and 24.3% PAE was achieved. Power density was 0.75 W/mm.



(a) 100-200-600 μm Amplifier



(b) 600-1200 μm Amplifier



(c) 1200-2400 μm Amplifier

Figure 39. Photographs of Ka-band amplifiers.

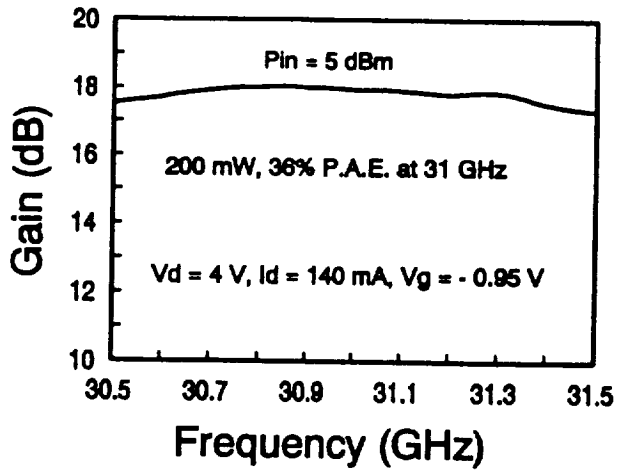


Figure 40. Performance of a three-stage 100-200-600 μm amplifier.

Using double pseudomorphic HEMT material (on 3 inch wafers) resulted in further progress. The first Ka-band amplifier wafer using PHEMT material had the following performance. Three-stage amplifiers (100-200-400 μm) achieved broadband performance with up to 200 mW output (20 dB gain) over 28 to 35 GHz. The efficiencies are in the 20s. With a slight output tuning, efficiencies greater than 30% can be achieved at 31 GHz. The optimum drain voltage was in the range of 4 to 5 V. The best amplifier achieved 200 mW output with 23 dB gain and 33.5% PAE at 31 GHz (with a drain voltage of 4.5 V). The gain is about 5 dB higher than our previous best amplifier using HFET material (at 200 mW output). The second stage of the 600-2 × 600 μm amplifier was also tested. With the first stage sawed off (with hybrid matching circuit in the input), the 2 × 600 μm stage achieved an output power of 680 mW with a record PAE of 37% (with 5.3 dB gain) at 31 GHz.

To show the possibility of using these amplifiers for low-noise receiver applications, we measured the noise figures of several three-stage amplifiers. The best amplifier had a 4 to 5 dB noise figure with ~30 dB gain at Ka band (at a drain voltage of 1.5 to 2 V). Considering that the device size and processing are not optimum for low-noise operation, these are good results. Thus, it is feasible to use PHEMT material for power and low-noise amplifier integration on the same GaAs substrate without requiring complex multimaterial structures or regrowth.

The next batch of 3-inch wafers in process was recessed using reactive-ion etching (RIE) with etch-stop layer. This resulted in record uniformity. The I_{dss} of one wafer had a standard deviation of 3.9%, and the other had 4.5%. The third wafer had enhancement-mode devices, as the etch-stop layer was too close to the InGaAs layer. The I_{max} standard deviation was 12.8%. At this time, amplifiers from the first 3-inch wafer have been evaluated and yielded record power/gain/efficiency performance.

A three-stage amplifier (100-200-400 μm gate widths) achieved an output power of 320 mW with 22 dB gain and 36% PAE at 31 GHz. The amplifier was biased at a 5 V drain voltage. At 320 mW output, the drain current was 177 mA. The quiescent drain current was about 20 mA. This low standby current is characteristic of near-Class-B, high-efficiency mode amplifier operation. Figure 41 shows the performance over the 30.5 to 31.5 GHz frequency band. With a reduced drain voltage of 4 V, the PAE increases to a record 40% with 235 mW output and 20.7 dB gain at 31 GHz. These results are summarized in Table 6. More than five amplifier chips were tested from this slice with essentially the same performance, indicating a high degree of uniformity across the slice because of the RIE recess with etch-stop layer.

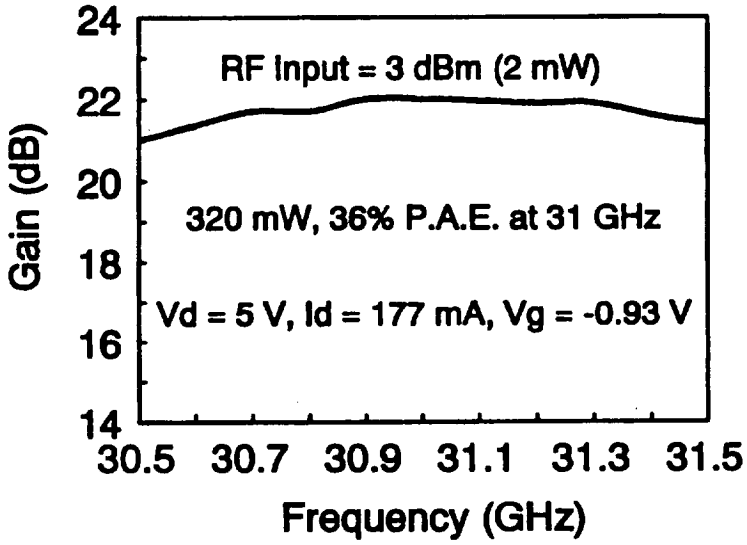


Figure 41. Performance of a three-stage Ka-band MMIC amplifier.

Table 6.
Performance at 31 GHz

Power (mW)	Gain (dB)	PAE (%)	V_d (V)	I_d (mA)	V_g (V)
320	22	36	5.0	177	-0.93
235	20.7	40	4.0	147	-0.93

In addition to power testing of amplifiers, we also performed on-wafer S-parameter measurements of various discrete devices (gatewidths 100, 200, 400, and 600 μm). Figure 42 and Table 7 show the modeled element values. These values were obtained by fitting measured S-parameters over the 0.1 to 40 GHz frequency range. Excellent agreement between the modeled and measured S-parameters was obtained, indicating good measured data. Figures 43 and 44 show, respectively, the current gain and power gain of 100 μm and 600 μm devices. The extrapolated unity current gain frequency f_t is around 50 GHz.

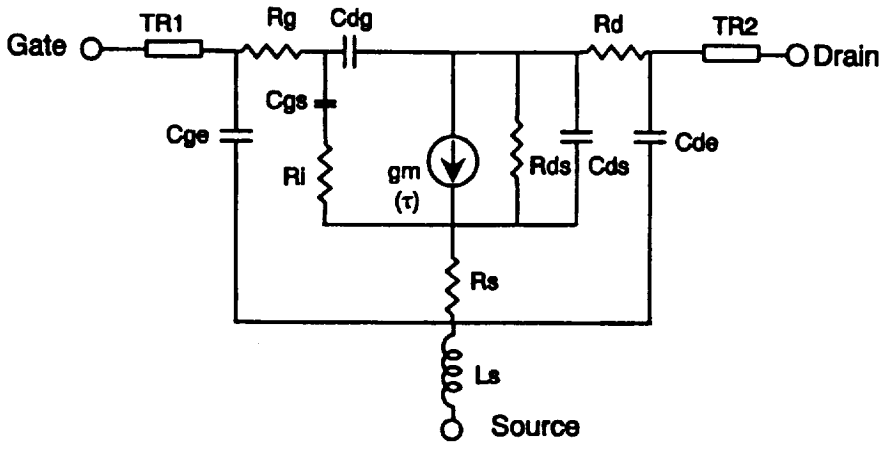


Figure 42. Modeled element values from PHEMT slice 210-697.

Table 7.
Device Model

Parameter	Gatewidth (μm)			
	100	200	400	600
R_g	1.52	1.06	0.78	1.29
R_i	2.99	1.77	0.97	0.3
C_{gs}	0.17	0.31	0.64	0.9
Cdg	0.01	0.026	0.051	202
g_m	51.8	102	1.46	1.22
τ	1.54	1.44	1.46	1.22
R_s	1.58	0.86	0.42	0.40
R_{ds}	483	245	123	84
C_{ds}	0.01	0.03	0.063	0.11
R_d	2.79	1.52	0.85	0.37
L_s	0.007	0.003	0.005	0.004
C_{ge}	0.001	0.001	0.003	0.003
C_{de}	0.033	0.024	0.027	0.007

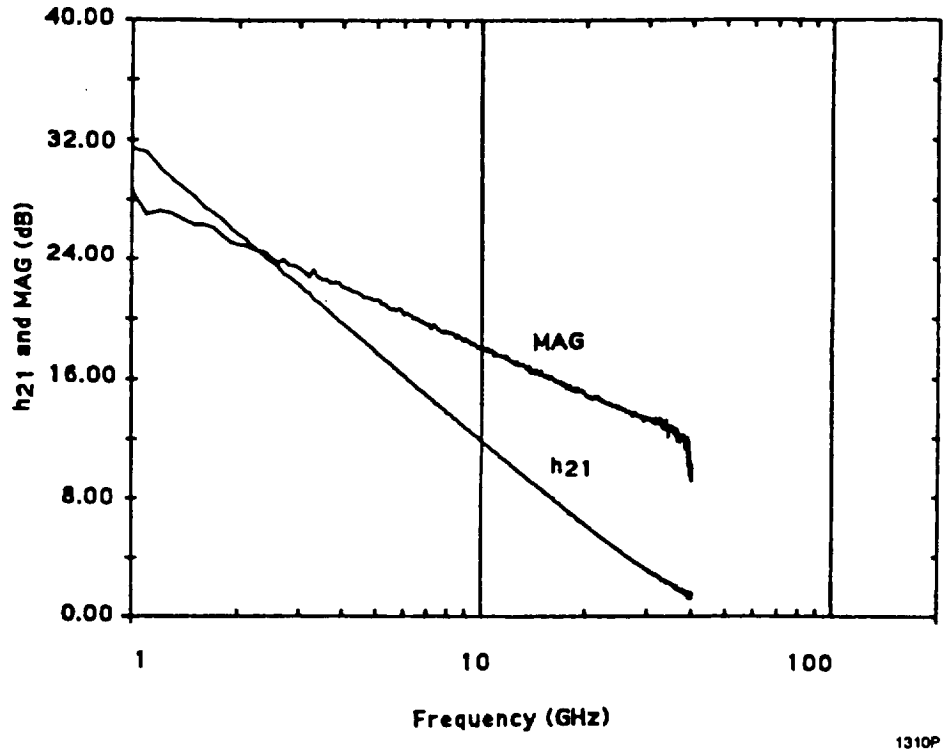


Figure 43. Small-signal gains of 100 µm gatewidth PHEMT.

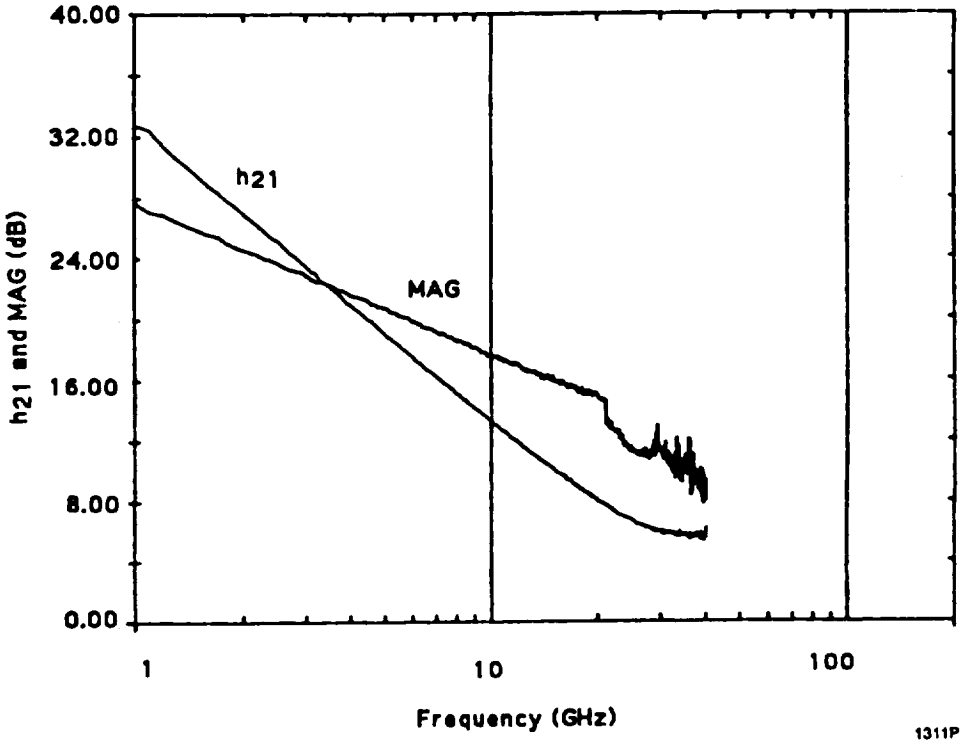


Figure 44. Small-signal gains of 600 µm gatewidth PHEMT.

A final batch of three wafers was processed. Two wafers were completed but a third wafer was ruined at lapping. The wafer with delta (non-T) gates gave better results than the T-gate wafer. Three three-stage amplifiers with 100, 200, and 400 μm gatewidth devices had the following performances at 31 GHz:

300 mW, 15.3 dB, 37% PAE
260 mW, 17 dB, 40.5% PAE
142 mW, 15 dB, 42.3% PAE (V_d = 3 V).

Although we obtained a record PAE, the gains were about 5 to 6 dB lower than those of our previous best wafer.

The lower gains of the three-stage amplifiers were traced to the differences in the gate voltages for peak transconductance for different device sizes (100-200-400 μm). The peak seems to shift toward zero gate voltage (less negative) as the cell size is reduced. The earlier wafer with etch-stop layer has devices with uniform peak transconductance at the same gate voltage. This results in a substantial gain increase (5 to 6 dB for the three-stage amplifier).

The big two-stage Ka-band amplifier (2 × 600 μm) still shows oscillation tendency in the 35 to 40 GHz frequency range. Several amplifiers were sawed and the first and second stages were tested. The first stage has very low gain, which also peaks at low (27 to 29 GHz) frequency. The last stage, however, worked very well and achieved an output power of 794 mW with 5 dB gain and 38.2% PAE. Maximum output power was 870 mW with 4.8 dB gain and 35.5% PAE.

We discovered that we had made a mistake in one of the interstage capacitors of the 600-1200 μm amplifier. It was laid out as 10 times smaller than we had designed it. Time constraints prevented correction of the error under this program, but a new corrected mask set is being fabricated under another program.

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Paul Saunier and Hua Quen Tserng

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13. ABSTRACT ***(Maximum 200 words)***

Over the course of this program, very extensive progress was made in Ka-band GaAs technology. At the beginning of the program, odd-shaped VPE MESFET wafers were used. A breakthrough in power and efficiency was achieved with highly doped (8×10^{17} cm^{-3}) MBE grown MESFET material. We obtained power of 112 mW with 16 dB gain and 21.6% efficiency at 34 GHz with a monolithic 50-100-250 μm amplifier. The next breakthrough came with the use of heterostructures grown by MBE (AlGaAs/InGaAs where the InGaAs is highly doped). This allowed us to achieve high power density with high efficiency. A benchmark 40% efficiency was achieved with a single-stage 100 μm MMIC at 32.5 GHz. The corresponding three-stage 50-100-250 μm amplifier achieved 180 mW with 23 dB gain and 30.3% efficiency. The next breakthrough came with 3-inch MBE grown PHEMT wafers incorporating an etch-stop layer for the gate recess (using RIE). Again, state-of-the-art performances were achieved: 40% efficiency with 235 mW output power and 20.7 dB gain. The single-stage 2 x 600 μm chip demonstrated 794 mW output power with 5 dB gain and 38.2% power-added efficiency (PAE). The Ka-band technology developed under this program has promise for extensive use: JPL demonstrated 32 GHz phased arrays with a three-stage amplifier developed under this contract. A variation of the three-stage amplifier was used successfully in a 4 x 4 phased array transmitter developed under another NASA contract.

14. SUBJECT TERMS

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